Circuit Design and Verification of 7nm Low-Power, Low-Jitter PLLs

Andrew Cole

VP Business Development

Silicon Creations, LLC

May, 2018

USER2USER

MENTOR USER CONFERENCE

Outline

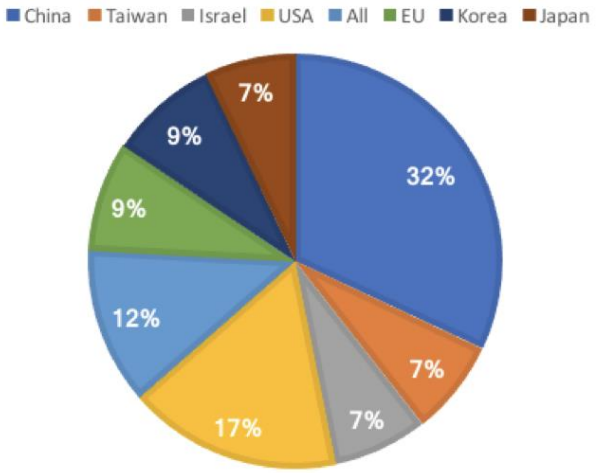
- Silicon Creations introduction
- Product overview
- Key PLL Specifications and Applications
- Introduction to PLL architecture and core building blocks
- Simulation benchmarking and Silicon Results
- Summary

Silicon Creations Overview

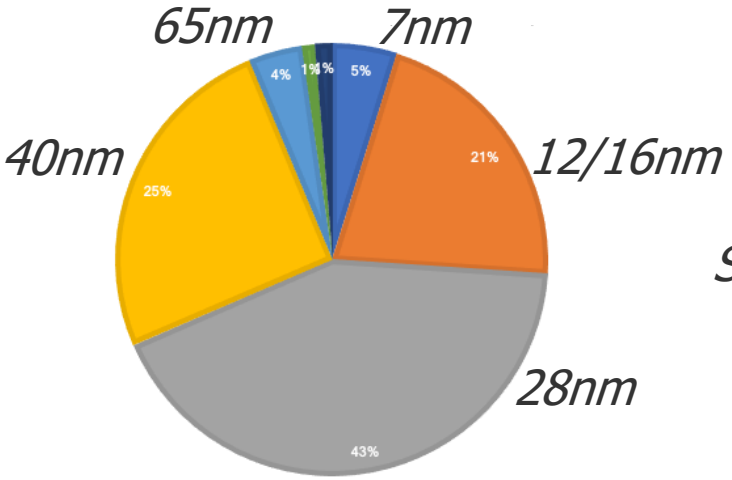
- IP provider of PLLs, Oscillators and High-speed Interfaces
- Founded 2006 – self-funded, profitable and growing
- Design offices in Atlanta and Krakow, Poland
- High quality development, award winning support
- >160 customers (>60 in China)
- Over 10 foundries, mass production from 7nm to >180nm, 5nm coming

PLL Sales

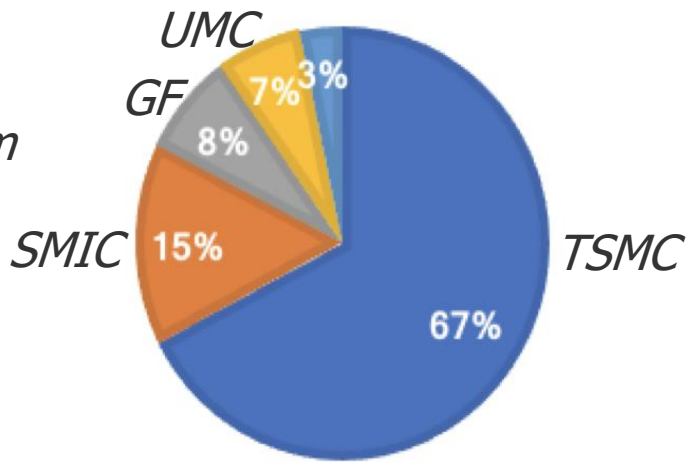
… by Region

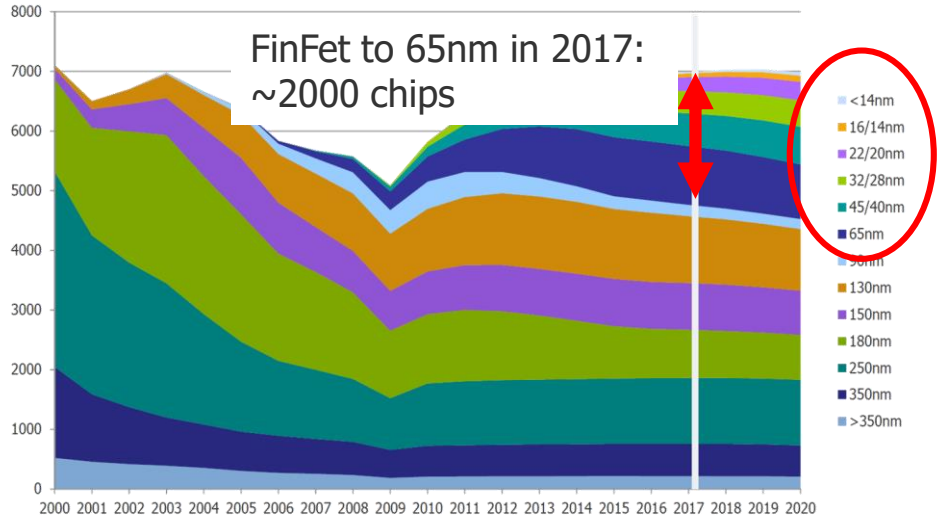


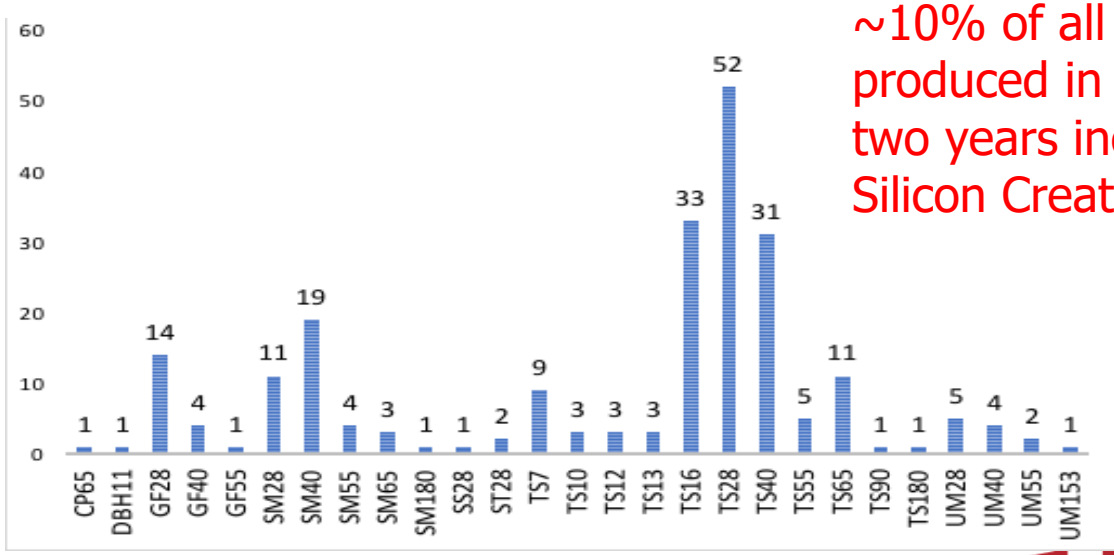
… by Node



… by Foundry







~10% of all chips produced in the last two years include a Silicon Creations PLL

Source: International Business Strategies, Inc. 2015

Awards for quality & support

TSMC

- 2017: Audience choice paper, USA OIP
- 2017: "Mixed-Signal IP Partner of the year"
- 2014: "Best Emerging IP vendor"

SMIC

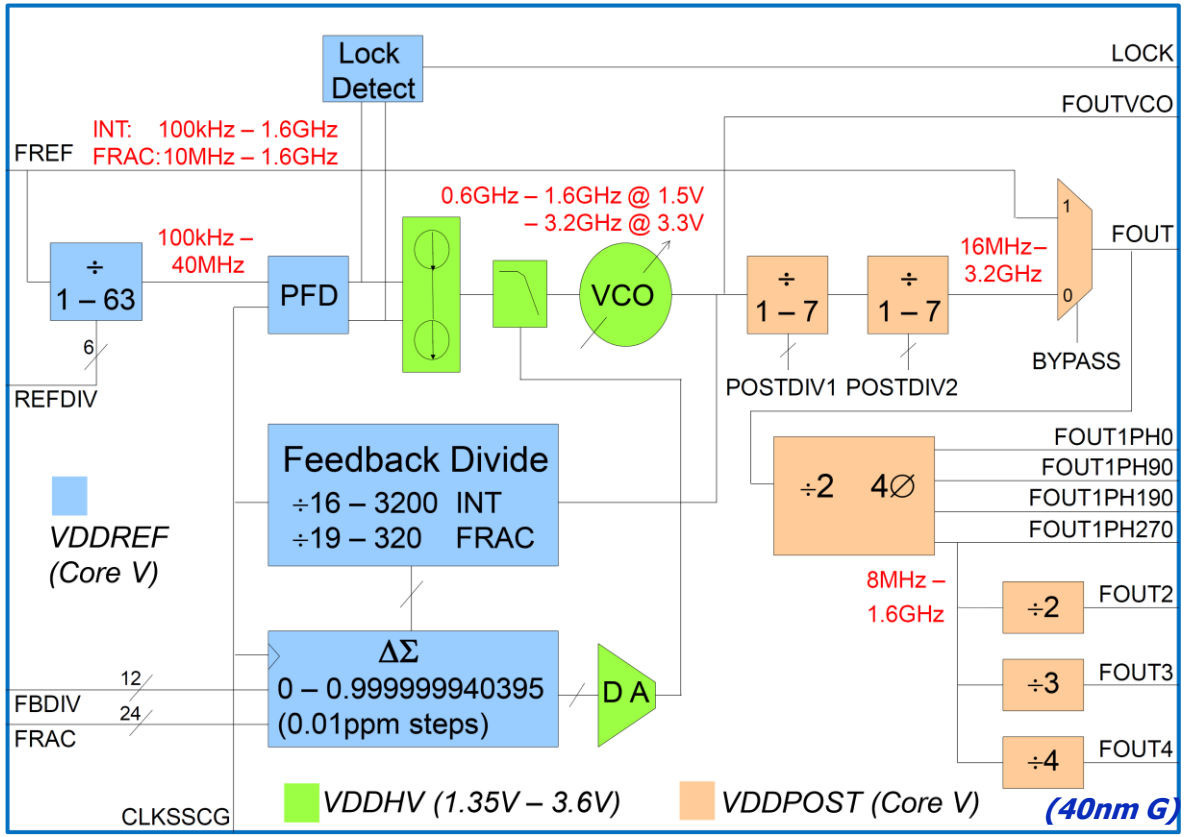
- 2017 (no awards to anyone)
- 2015 & 2016: Best support
- 2014: Production volume growth
- 2013: Best Analog IP

Outline

- Silicon Creations introduction
- Product overview
- Key PLL Specifications and Applications
- Introduction to PLL architecture and core building blocks
- Simulation benchmarking and Silicon Results
- Summary

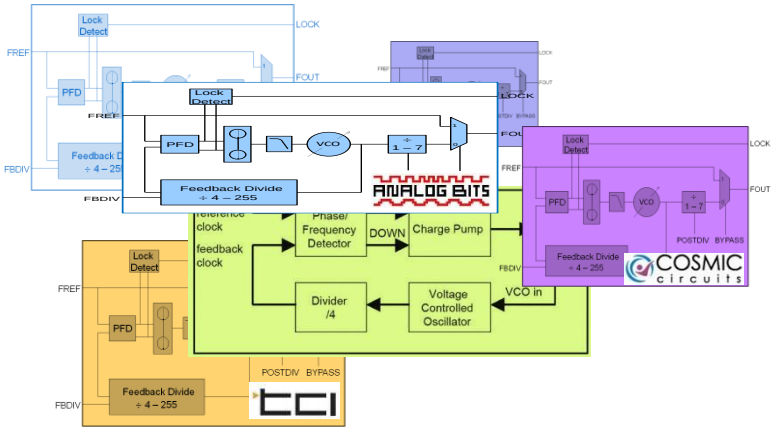
Fractional Ring PLL

- "One-Size-Fits-All" Synthesizer: flexibility reduces risk
  - Any crystal; <0.01ppm frequency step
- Programmable Power – Jitter Optimization
  - < 1mW
  - Long Term Jitter < 5ps RMS
- Production from 7nm, 5nm in development
- Derivative PLLs for
  - Core voltage only
  - Integer-only
  - Low area
  - Ultra-low jitter
  - Ultra-low power



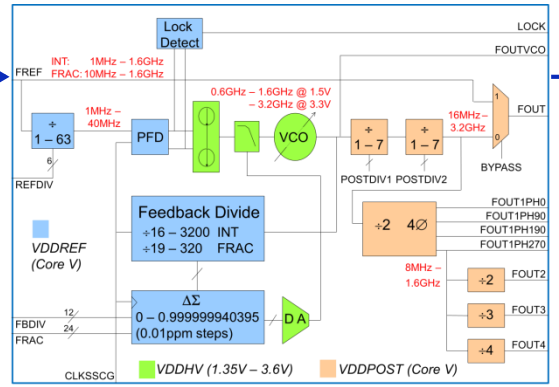
Why our Fractional PLL?

Competitor PLLs



Silicon Creations

1 to 1600 MHz



4 to 3200 MHz

Risky & expensive

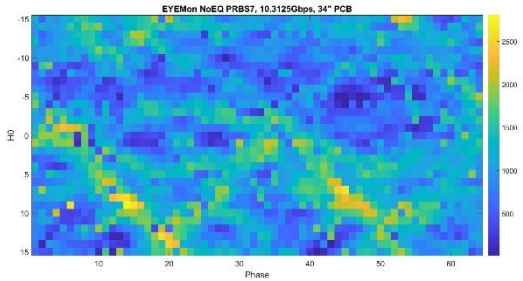
– Built new each time
– Narrow input/output ranges
  … new silicon to change
– Buy a new IP for every clock

Lower risk & lower cost

– Predictable, measured
– Wide range, programmable
  power-performance tradeoffs
– One PLL, many applications – save $, ¥, €
– Best support

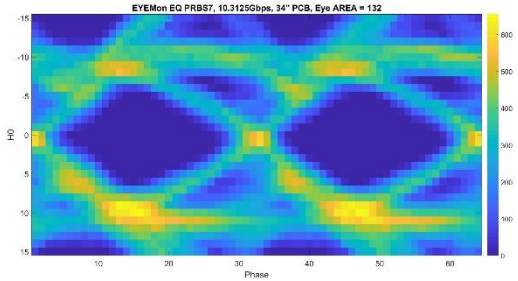
Multi-Protocol SerDes PMA

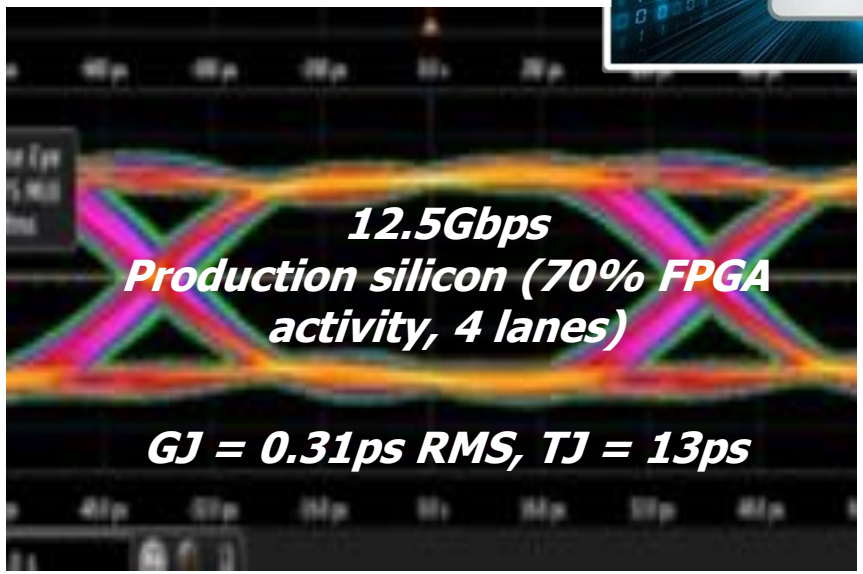
- 0.25 – 12.7Gbps SerDes PMA (28nm LP, 40 LP, 12FFC soon)
- Low Power (mW/Gpbs/lane): SR ~4.5mW, LR ~8.6mW
- Jitter cleaner Tx Ring PLL → Low Area



(10.3Gbps,
25dB channel loss)

5-tap DFE + CTLE +
Eye monitor +
Adaptive Eq.
→ **>30 protocols**





Outline

- Silicon Creations introduction
- Product overview
- **Key PLL Specifications and Applications**
- Introduction to PLL architecture and core building blocks
- Simulation benchmarking and Silicon Results
- Summary

One architecture can be optimized for…

Base Station

Ultra-Low Jitter

Data Center

Mobile

Mission Critical Long-term Reliability

High Frequency

Jitter-Power Optimized

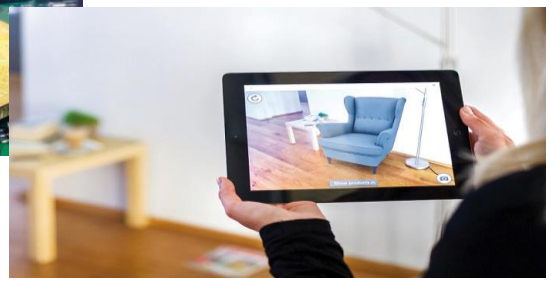
Autonomous Driving

Ultra-Low Energy

Area Optimized

Ultra-Low Power

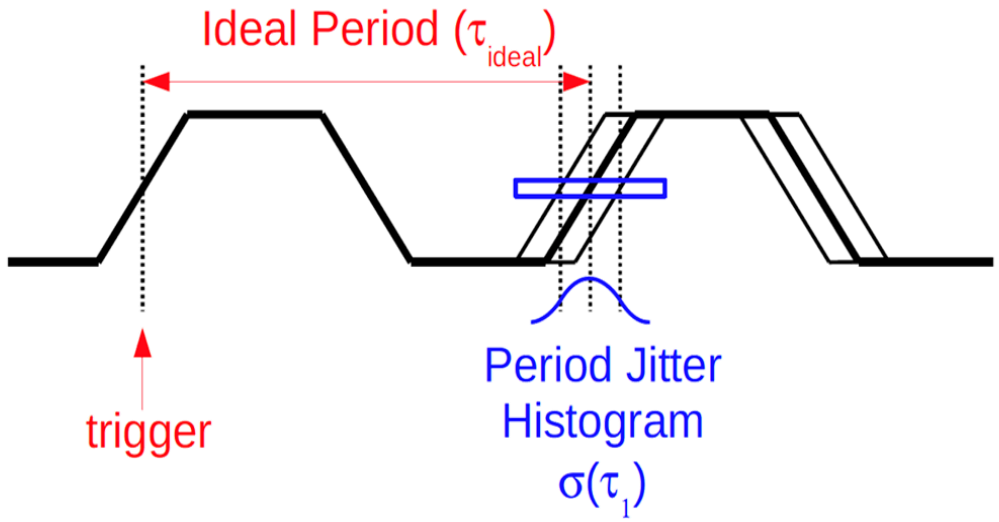
Bitcoin Mining

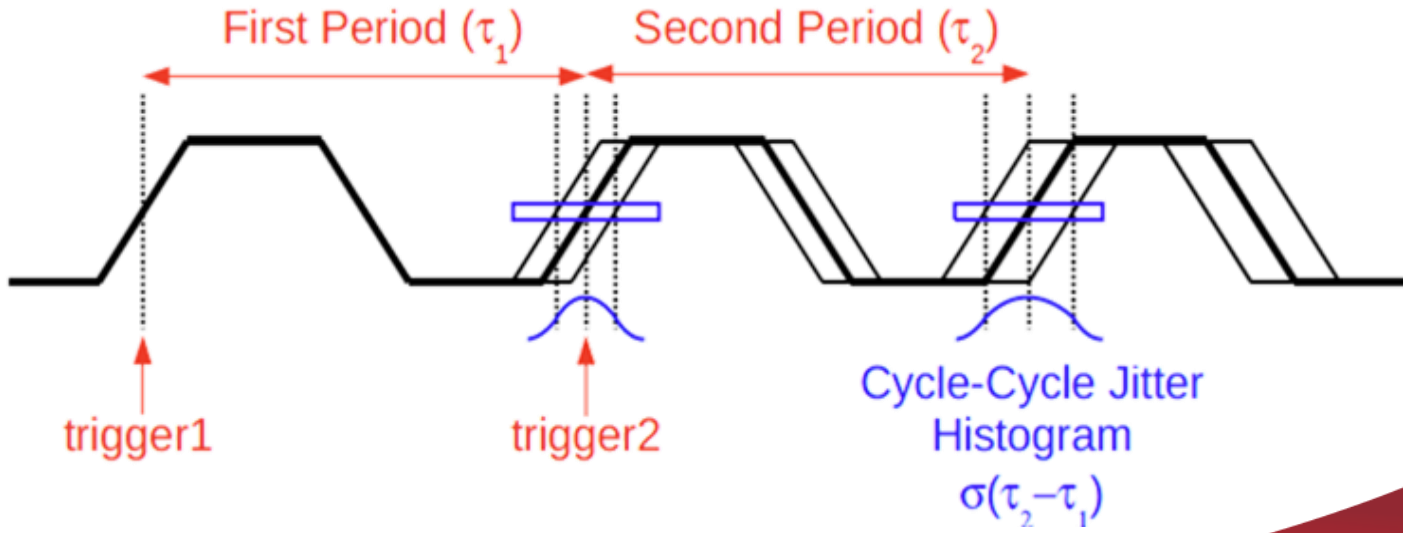


AI

Period Jitter (PJ) and Cycle-to-Cycle Jitter (CCJ)

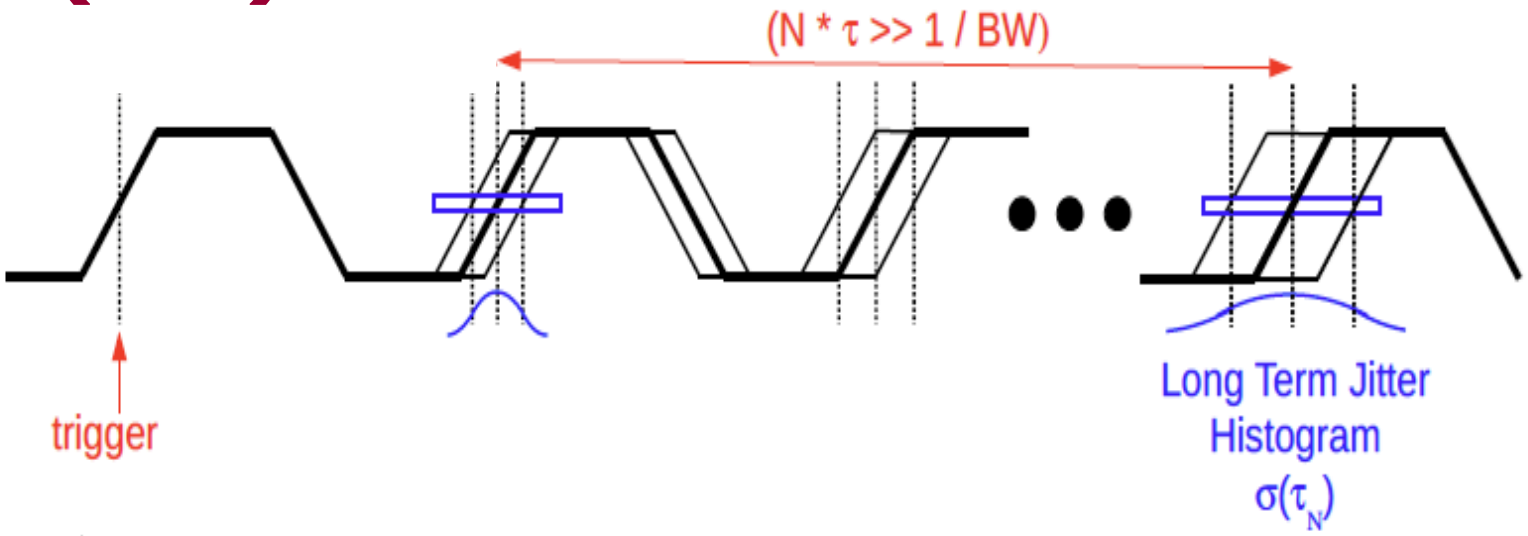
- Typically measured over 10k clock samples
- PJ
  - Variation of individual clock period length
  - Timing uncertainty for digital clocking (minimum & maximum possible clock period)
- CCJ
  - Variation of consecutive clock periods
  - Proxy for PJ for applications that require frequency modulation (e.g. Spread Spectrum)

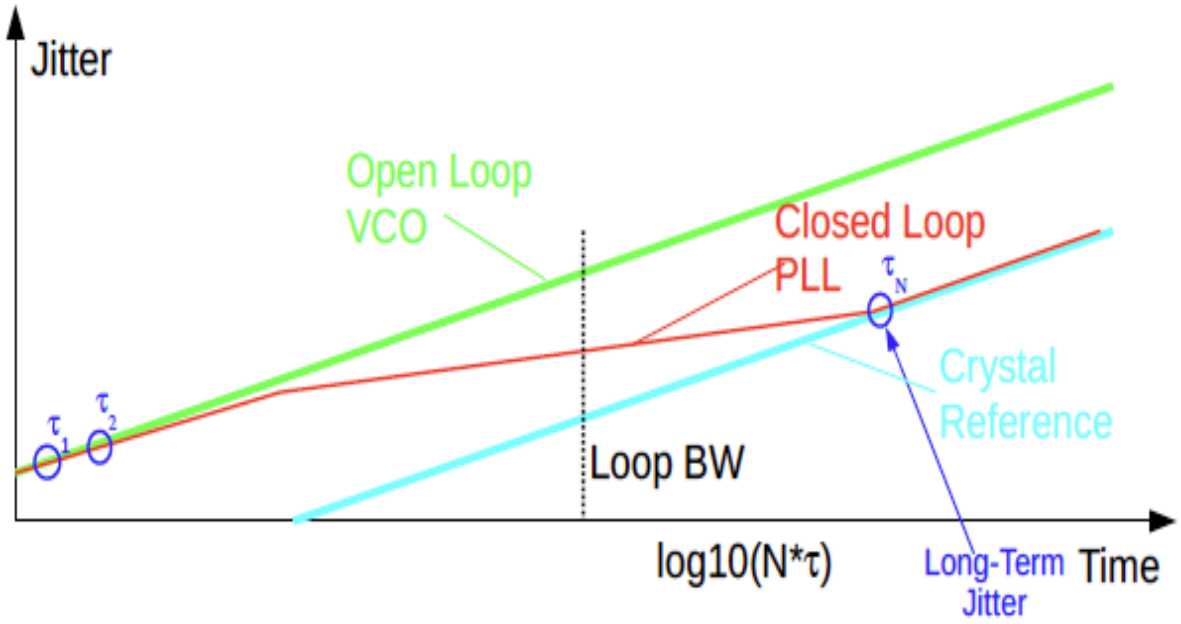




Long Term Jitter (LTJ)

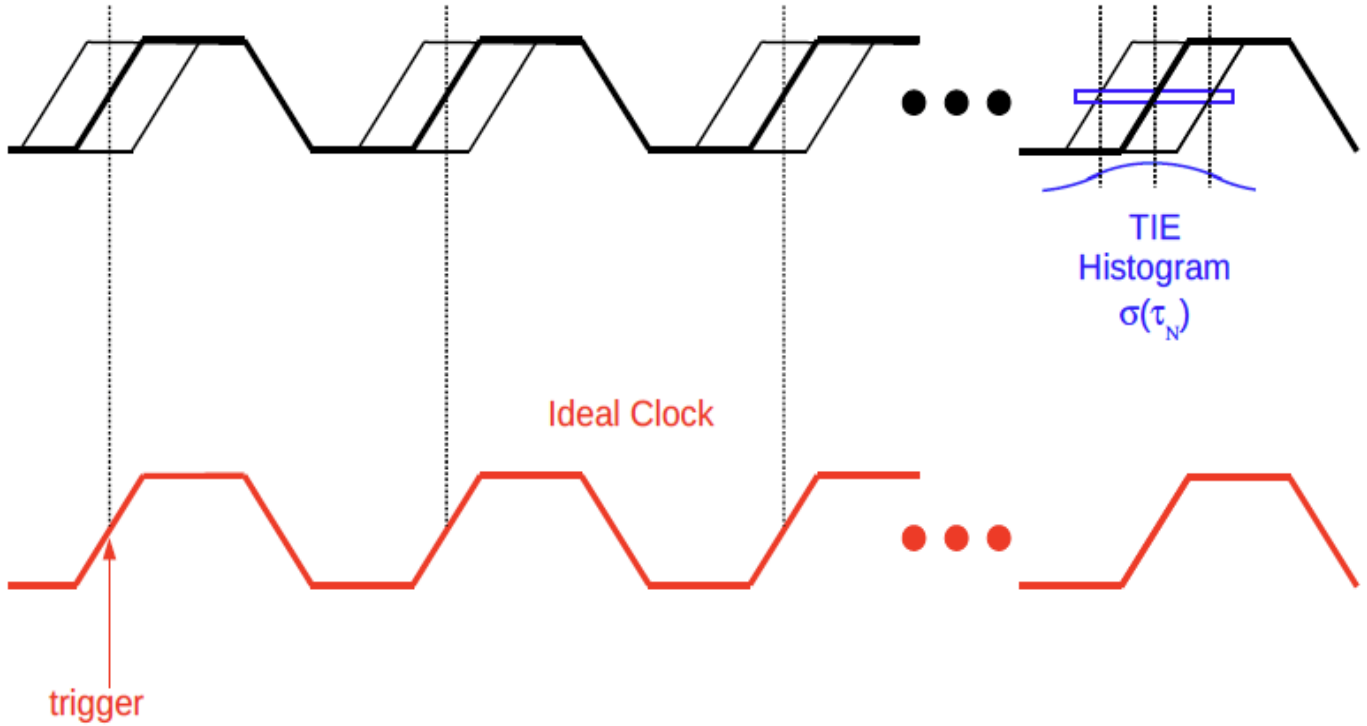
- Measures variation of clock phase (i.e. the integral of clock period)
- Measured at a hold-off time of several loop time constants
- Important for serial data links, data converters (ADC/DAC), asynchronous digital clocking





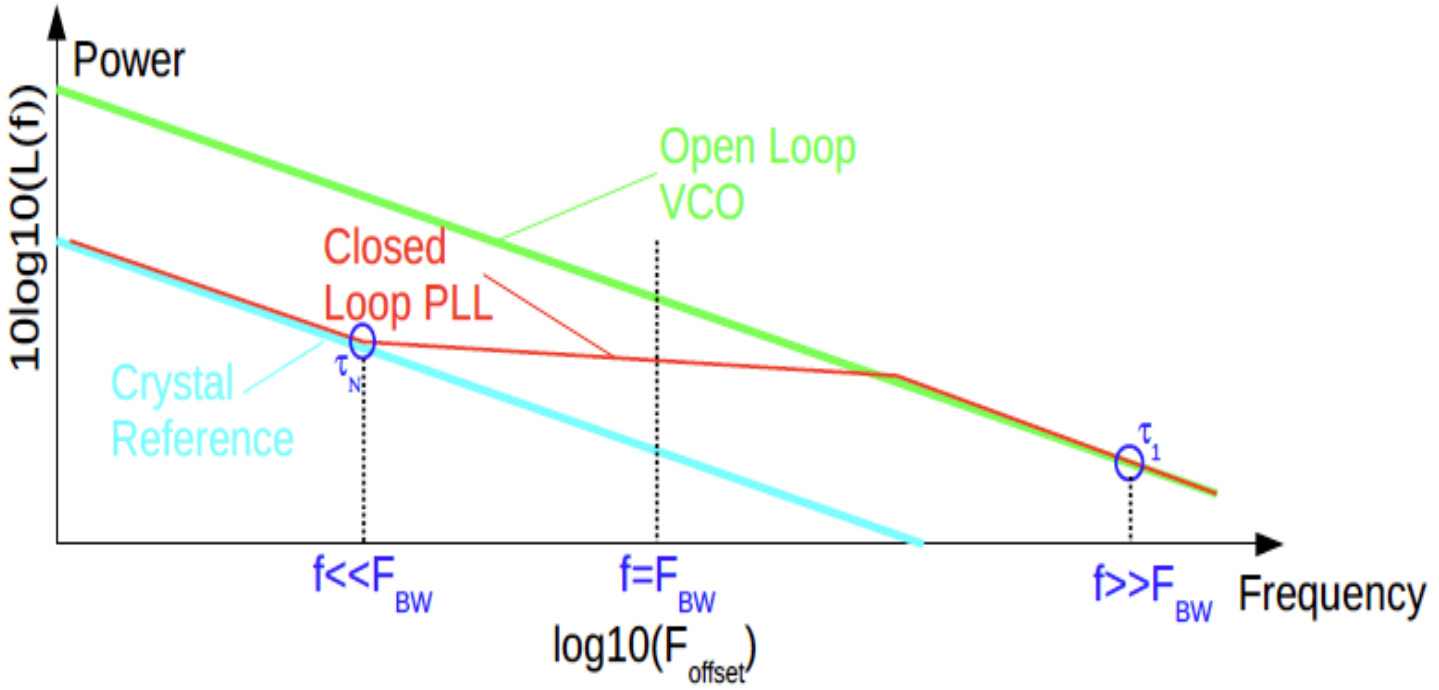
Time Interval Error (TIE)

- Measures variation of clock phase relative to an "ideal" clock
- "Single-sided" equivalent of LTJ
- Measurement bandwidth is determined by the application and can be set on the oscilloscope
- Important for serial data links, data converters (ADC/DAC), asynchronous digital clocking



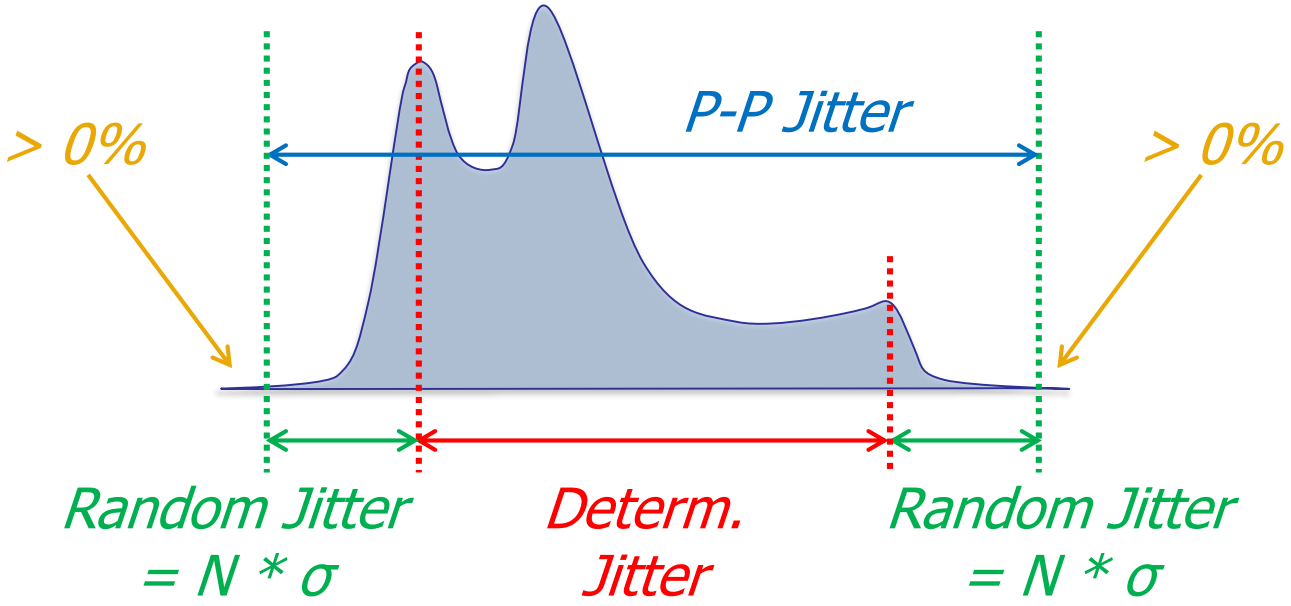
Phase Noise (PN)

- Measures power spectral density (PSD) of the clock signal relative to the ideal carrier
- Single-sideband PN is the frequency-domain equivalent of TIE
- Jitter is calculated by integrating the phase noise (across a specified band) and scaling by the clock period
- Important for RF communications, serial data links, data converters (ADC/DAC), asynchronous digital clocking



Statistics

- ”Peak-to-peak” jitter is calculated based on an appropriate σ value for random components (RJ) and then adding in bounded deterministic components (DJ)
- Random noise is unbounded and must be described statistically
- DJ comes from
  - Supply noise & coupling (usually dominant)
  - DCD
  - Mismatch

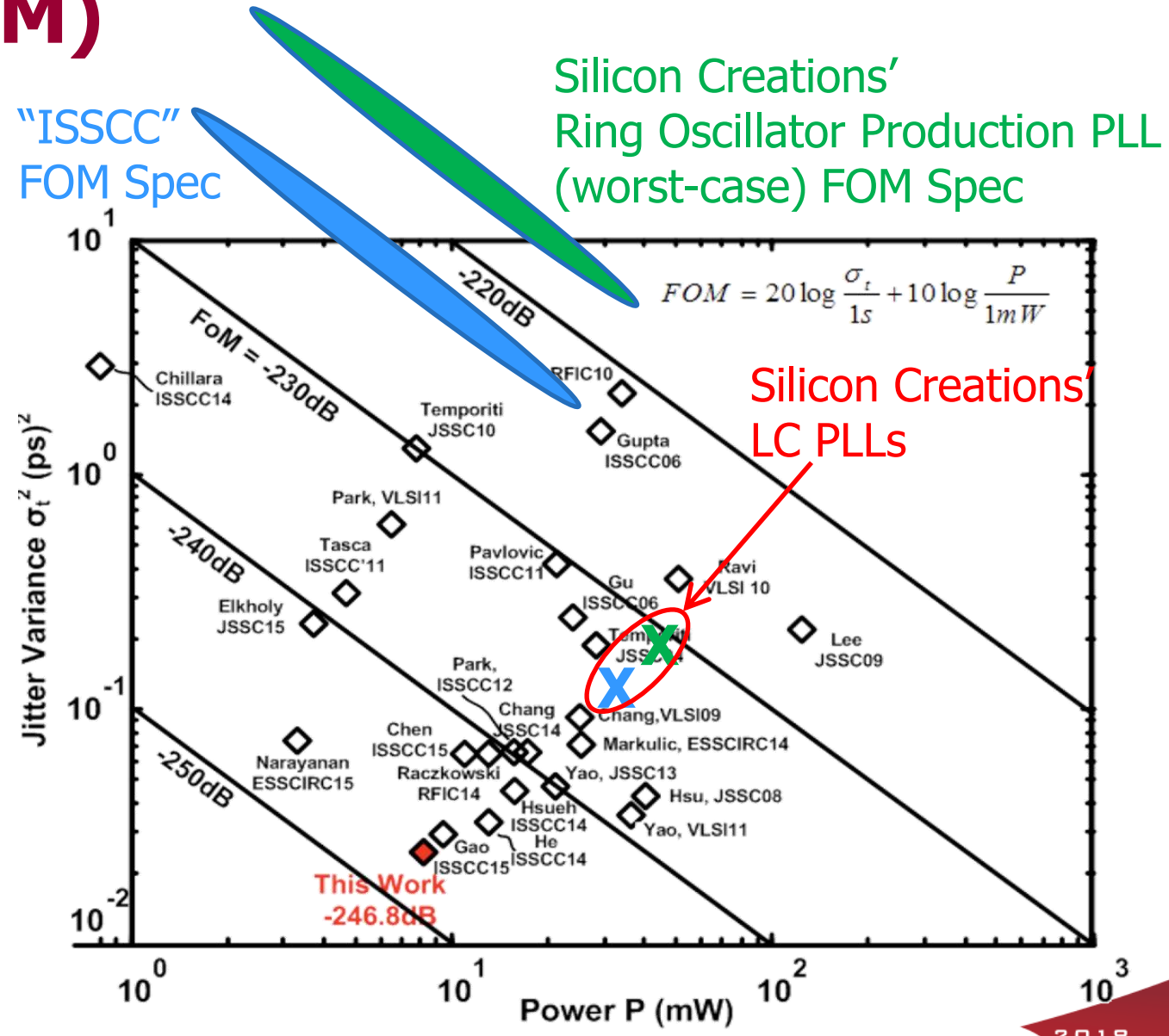


± N * σ	P-P probability
±1.0	68.3%
±2.0	95.5%
±3.0	99.7%
±7.0	100% – 1.0E-12
±7.9	100% – 1.0E-15

PLL Figure of Merit (FOM)

- Most reported PLLs use inductor-based VCOs
- Reported under ideal conditions, area = don't care, and not in production
- Example Silicon Creations ring oscillator PLLs:

Type	WC LTJ (ps RMS)	Power (mW)	FOM (dB)
Jitter Optimized fractional	2.4	40.1	-216
General-purpose fractional	3.9	12.9	-217
Core voltage digital clocking	9.9	1.9	-217
32kHz IoT (low energy)	3300	0.08	-180

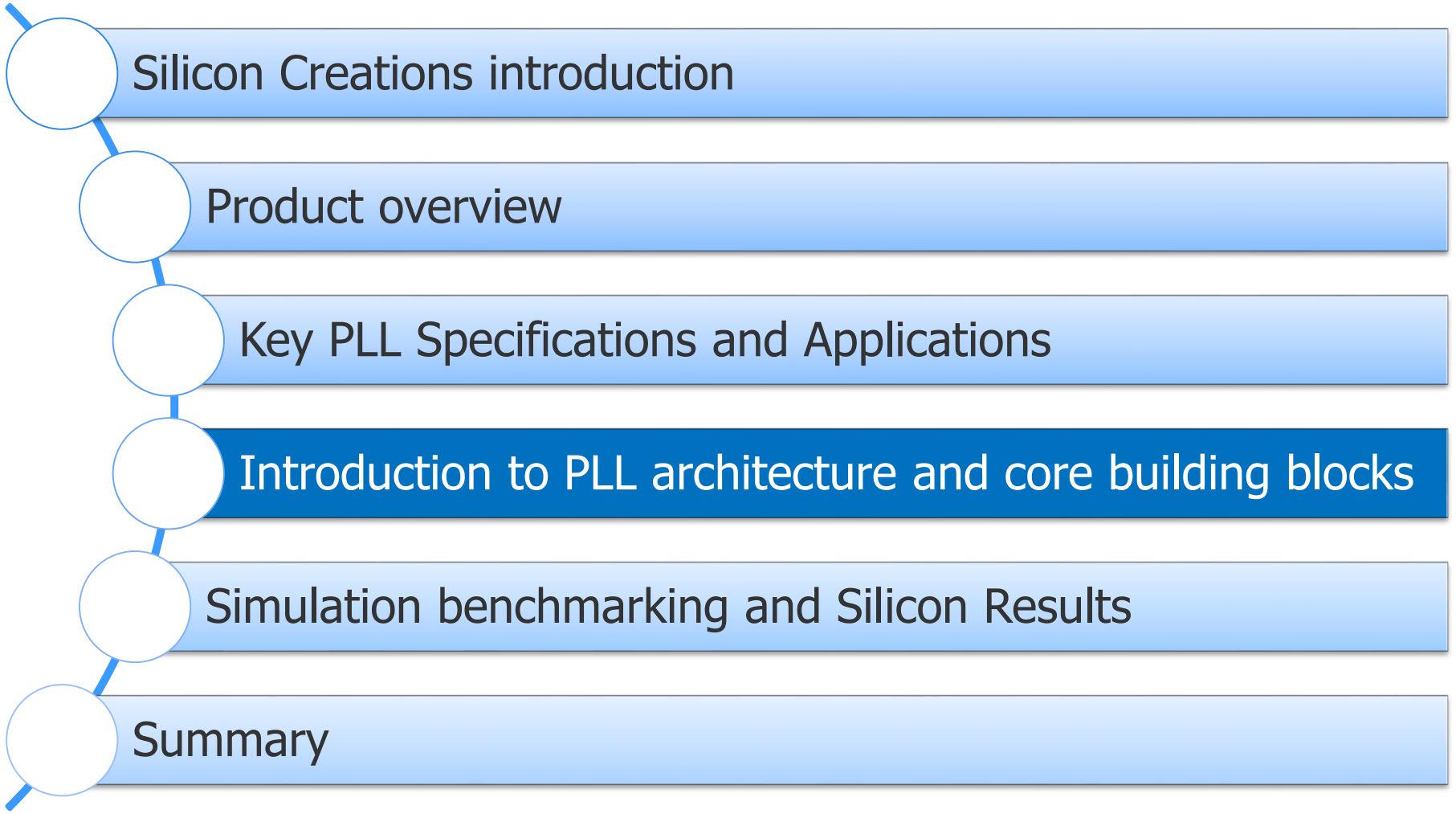


Source: ISSCC 2016/Gao: A 2.7-to-4.3GHz, 0.16psrms-jitter, −246.8dB-FOM, digital fractional-N sampling PLL in 28nm

Summary of key specifications

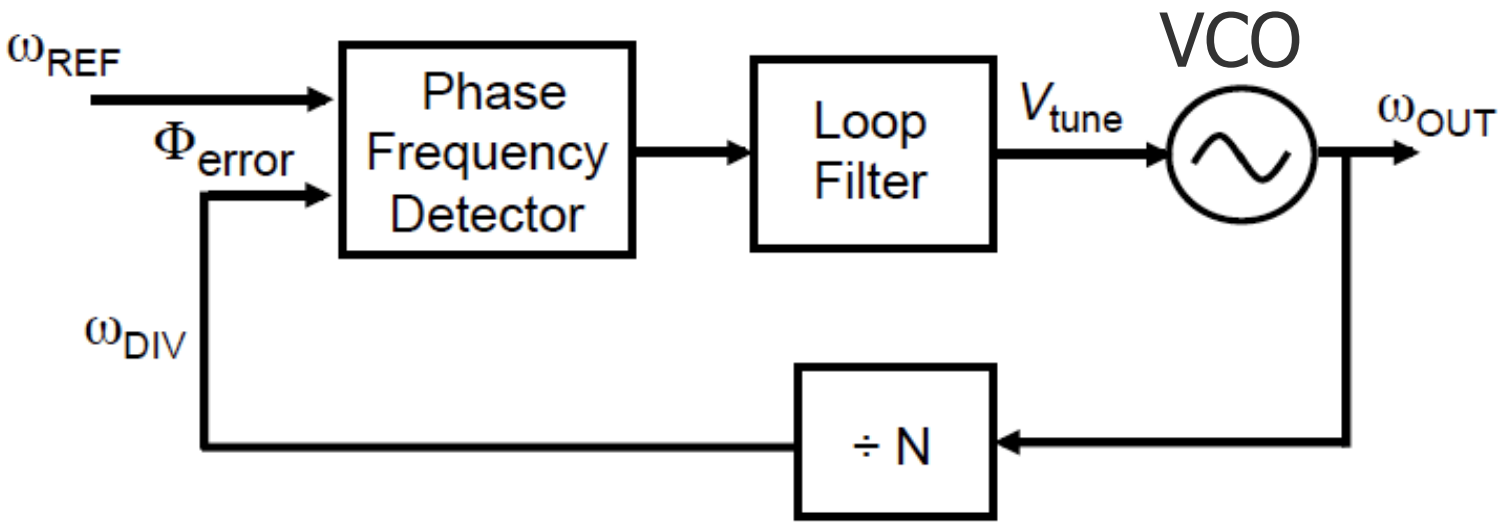
- Jitter is a key performance parameter. Need to know what matters in each case:
  - PJ for digital timing
  - LTJ for data converters and serial data
  - Phase noise for communications (not all bandwidths matter)
- Jitter has deterministic (bounded) and random (unbounded) portions – statistics matter
- Important to consider yield, area/cost and use case when comparing specs – FOM can lie

Outline



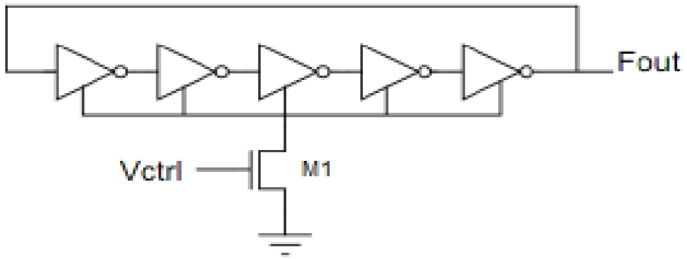
Standard PLL Block Diagram

- A feedback system that forces a given phase relationship between the reference (REF) edges and the VCO edges
- REF signal is usually obtained by a very stable, low-jitter crystal oscillator
- In-lock ωREF= ωDIV= ωOUT/N and the phase error Φerror is constant.

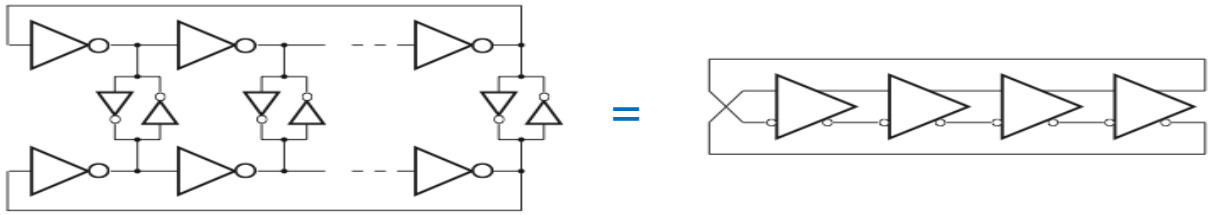


Source: "DTC-Based Digital PLLs" Carlo Samori, Politecnico Milano, Italy

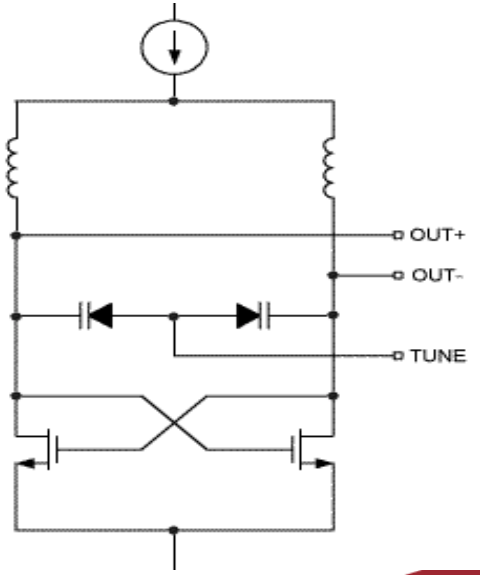
VCO Architectures



Single-ended, Current-starved, odd-stage ring oscillator
- Best FOM for ring oscillators
- Single-phase output only
- Guaranteed oscillation
- Wide frequency tuning range



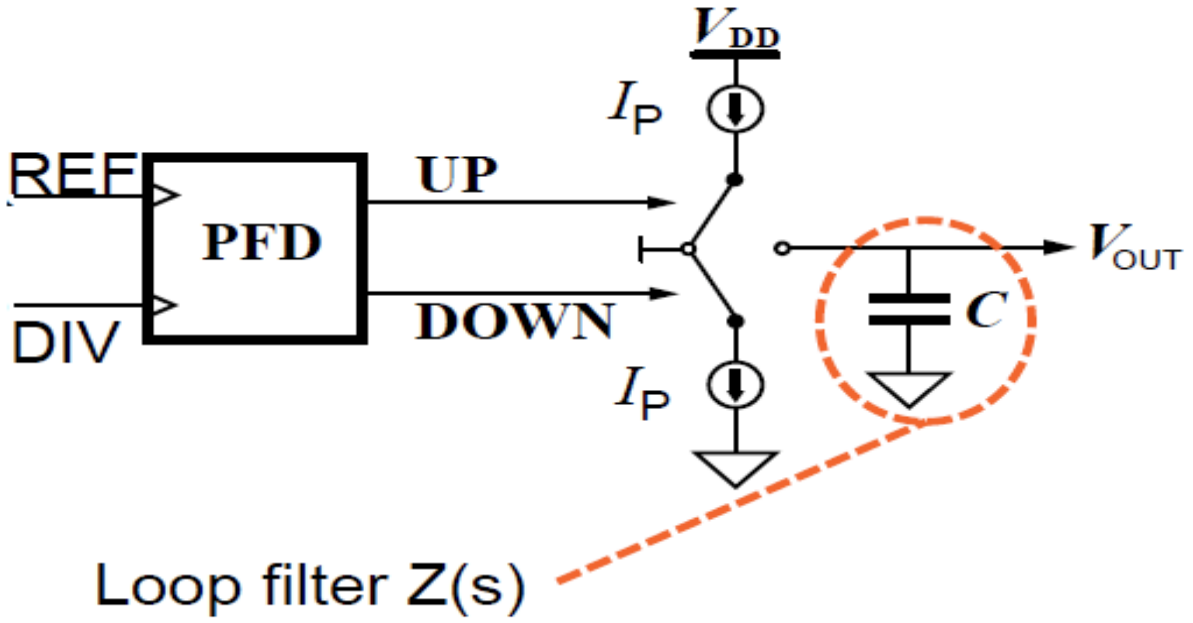
Pseudo-differential, Current-starved ring oscillator
- More current to achieve same jitter performance
- N*2-phase outputs are possible
- Two possible oscillation modes (only one is desired), needs positive feedback



Inductor-based "LC Tank"
- Better FOM compared to ring
- Narrow tuning range, may need calibration
- Large area due to inductors

UP/Down Control

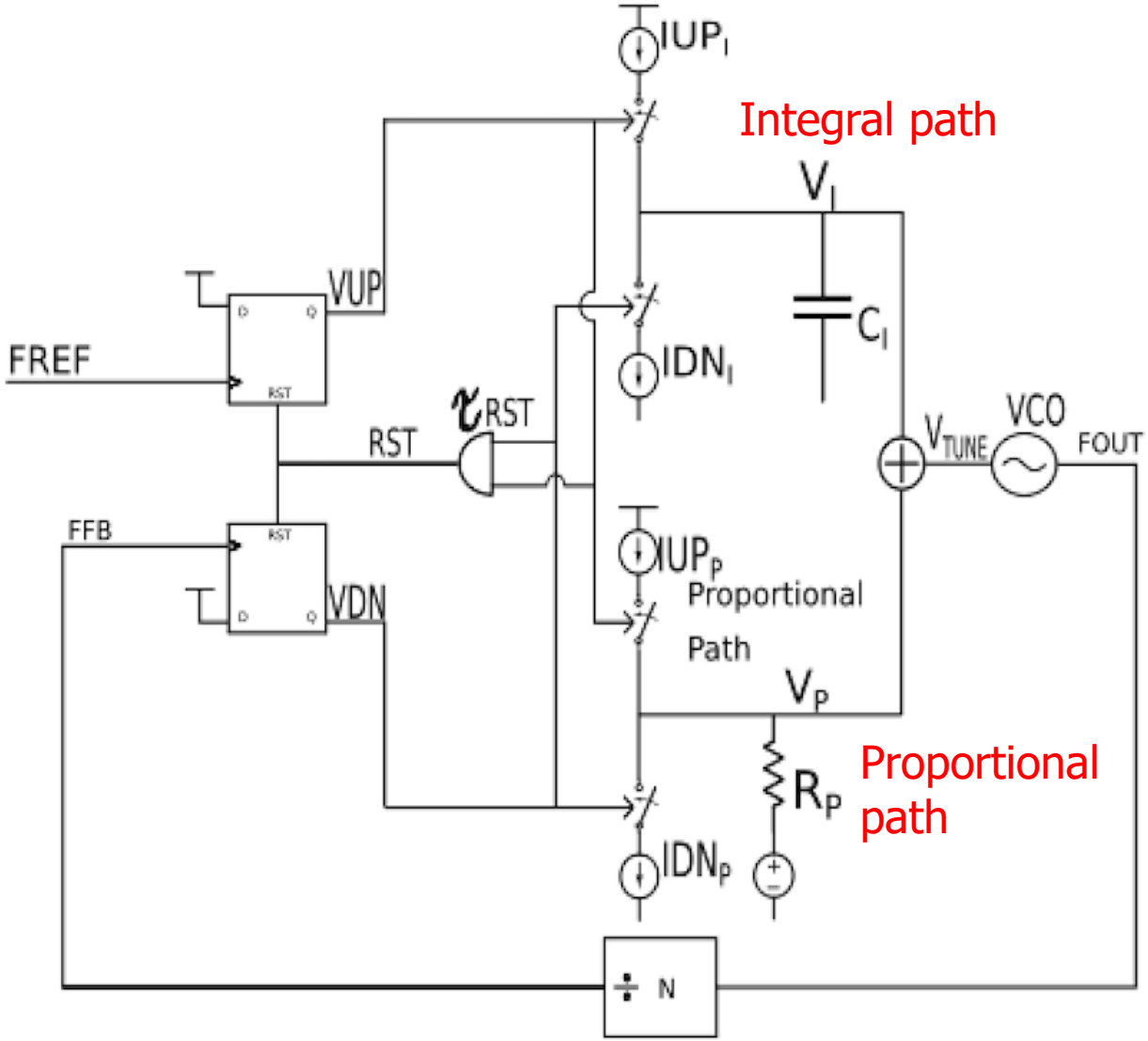
- In lock, the net charge onto the loop filter must be zero
- If there is mismatch between UP and DOWN currents, the loop will settle with a static phase offset (SPO) enabling the smaller current source to start earlier to match total charge
- SPO can result in large phase corrections on each reference edge, increasing the total jitter



Source: "DTC-Based Digital PLLs" Carlo Samori, Politecnico Milano, Italy

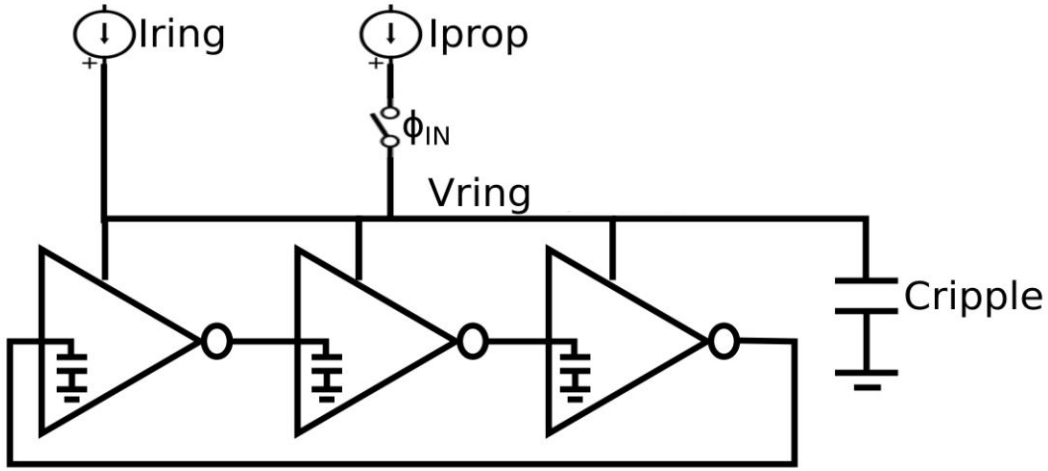
2-Path PI PLL

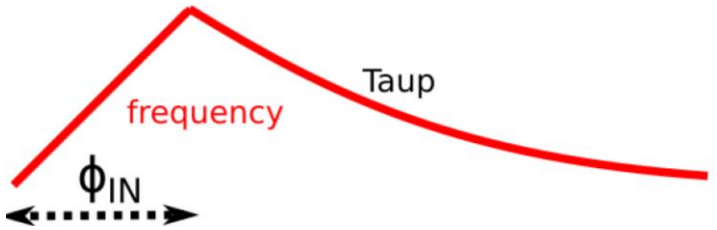
- Frequency is integrated to convert to phase in the VCO
- An additional integrator is realized by the current forced on the capacitor
- This solution makes the loop unstable, since it has two poles at DC (the CP one and the VCO intrinsic integration)
  - An additional zero must be added for stability
- A parallel charge pump can be added driving a resistor, which creates a "proportional" phase correction, with no memory



Proportional Correction

- One PFD (phase comparison) → integral and proportional charge pumps have the same Static Phase Offset (SPO) … can be auto-calibrated
- The proportional charge pump impacts the frequency immediately, causing a step in the VCO frequency
- A second capacitor (the "ripple cap") can be added to limit the frequency step (and limit the period jitter)
- The ripple cap size must be limited, since if it's too large, there will be memory from one reference edge to the next, and phase margin will be degraded

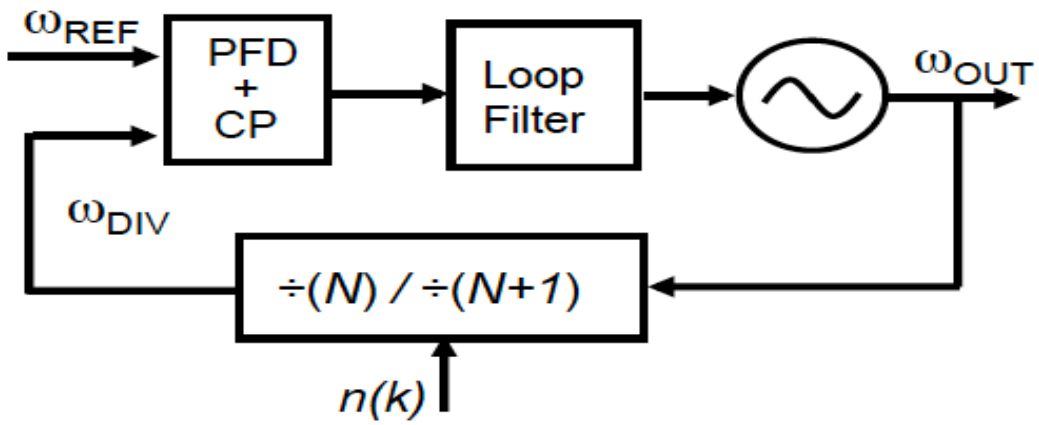


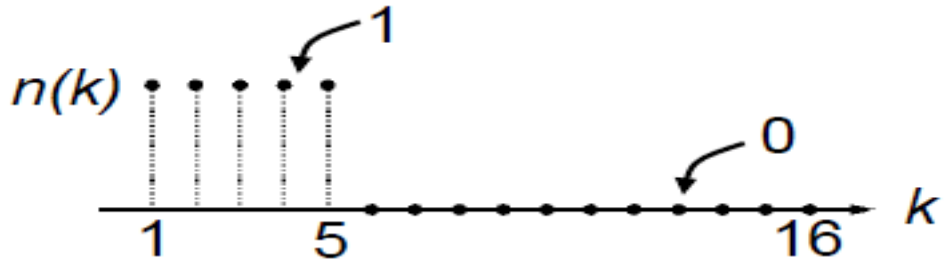


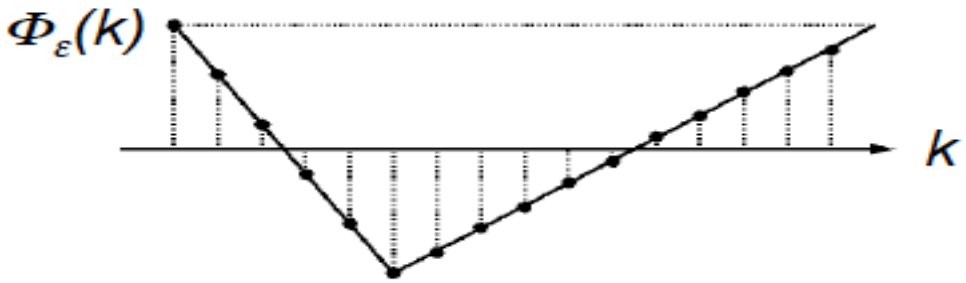
Source: "DTC-Based Digital PLLs" Carlo Samori, Politecnico Milano, Italy

Fractional PLL

- Feedback divide value can be changed dynamically to achieve a non-integer multiplication on average
- E.g. if we wish to divide by 5/16, we add 1 to the lower divide value for 5 out of 16 input clock cycles
- Fractional quantization error is shown as Φε(k)
- Disturbance (spur) in the output at Fvco/16 … reduced by mixing -2, -1, 0, +1 and +2 counts in a pseudo-random manner for same average
- Most of the quantization error is suppressed by the loop filter
- Remaining spurs are cancelled in Silicon Creations' PLL using a DAC to feed forward complementary pulses







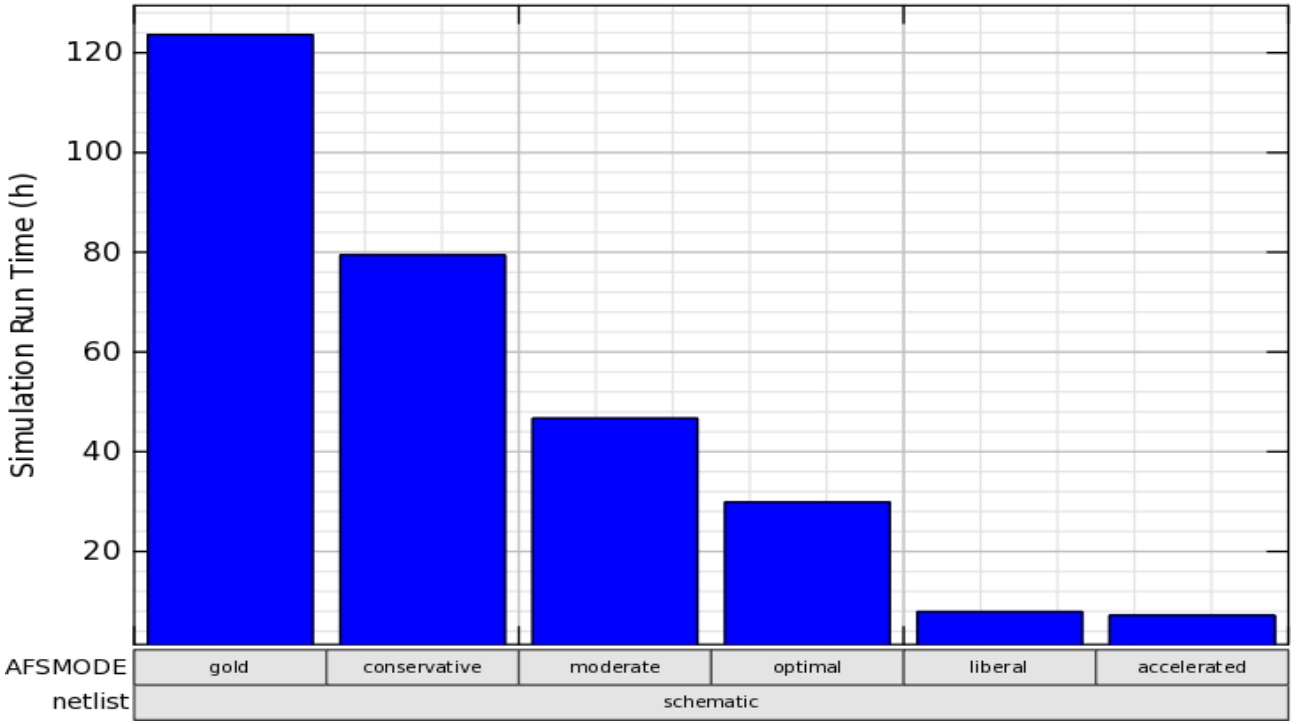
Summary of PLL architecture

- Current mode PLL design is well known, matches ring oscillator which is a current mode circuit
- Mismatch in charge pump and PFD causes SPO
- Dual path (proportional and integral) allows independent optimization of loop characteristics
- Fractional multiplication is very useful, and can be low jitter with spur correction

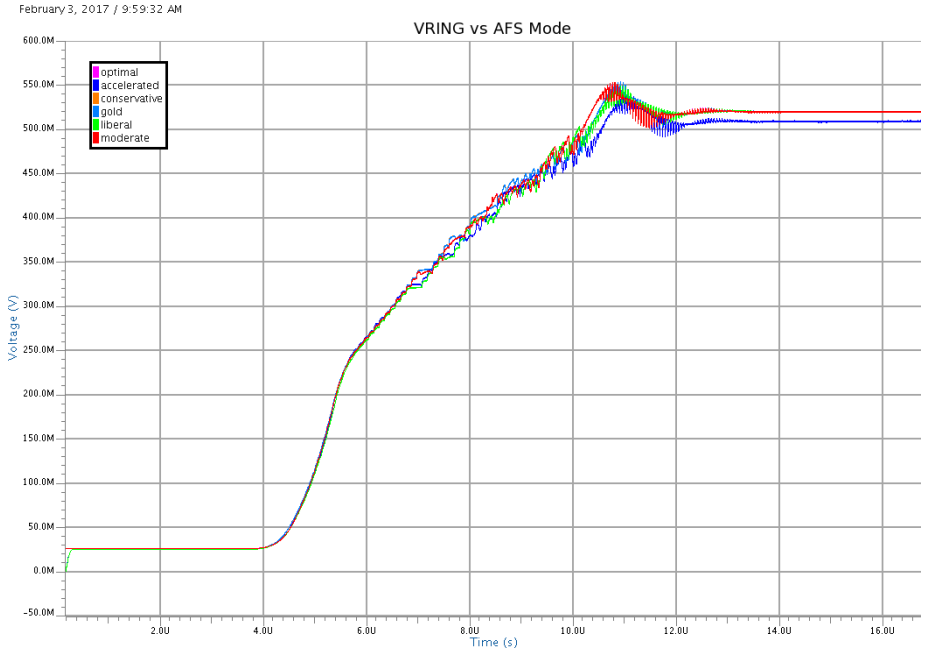
Outline

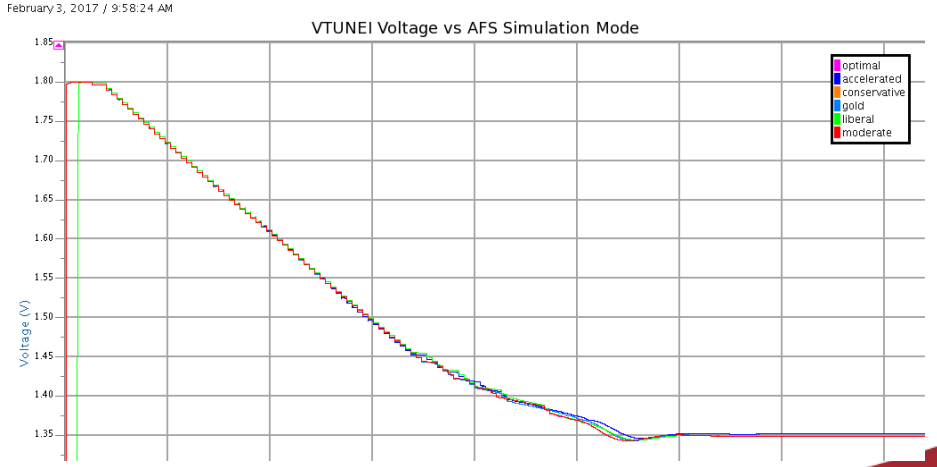
- Silicon Creations introduction
- Product overview
- Key PLL Specifications and Applications
- Introduction to PLL architecture and core building blocks
- Simulation benchmarking and Silicon Results
- Summary

Speed & Accuracy vs AFS Mode



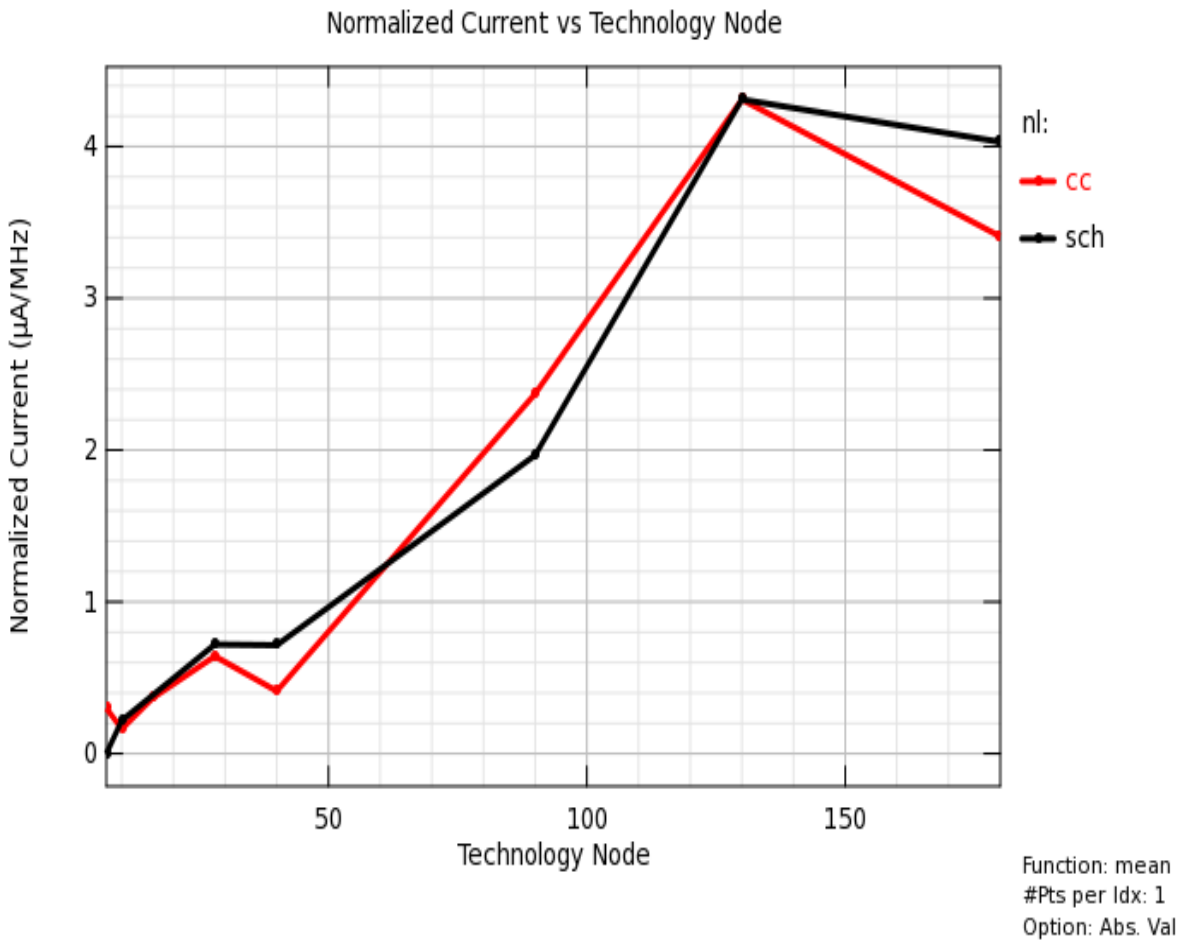
AFSMODE	Days	HMS	Total_H	Total_M	Total_S	netlist
gold	5	03:37:46	123.63	7417.77	445066	schematic
conservative	3	07:25:13	79.42	4765.22	285913	schematic
moderate	1	22:41:37	46.69	2801.62	168097	schematic
optimal	1	05:52:36	29.88	1792.60	107556	schematic
liberal	0	07:54:55	7.92	474.92	28495	schematic
accelerated	0	07:10:07	7.17	430.12	25807	schematic



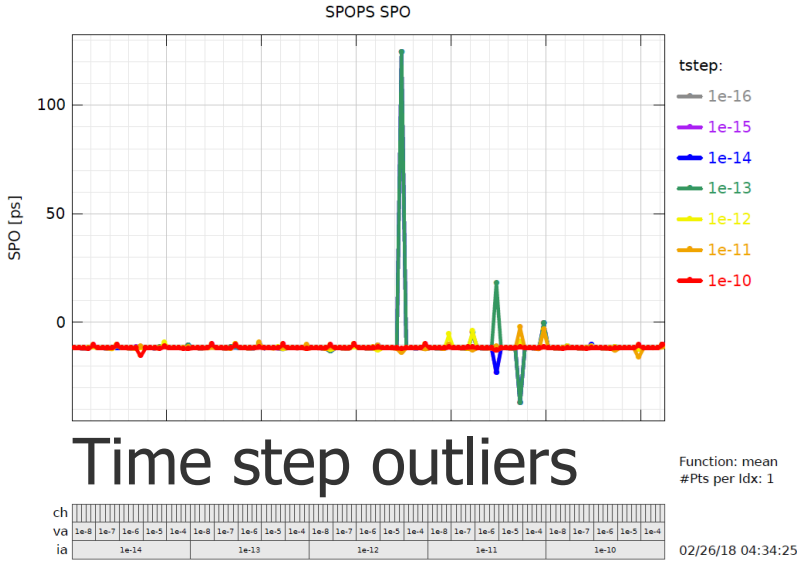


Current vs. Process node

- PLL core current consumption scales ~ as the square of the feature length
- From 40nm to 28nm (last planar node) the scaling leveled out, but resumed in the FinFET processes
- CC-extracted and schematic results show good correlation across all geometries



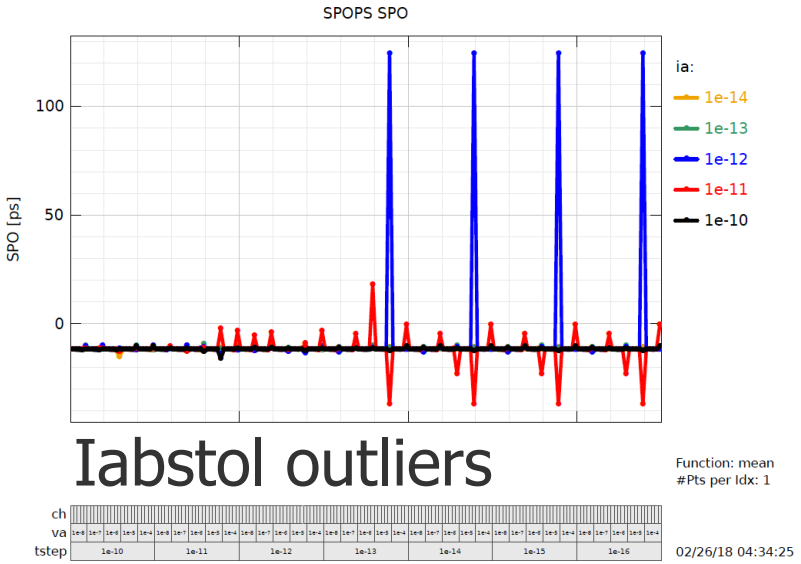
Charge Pump Linearity



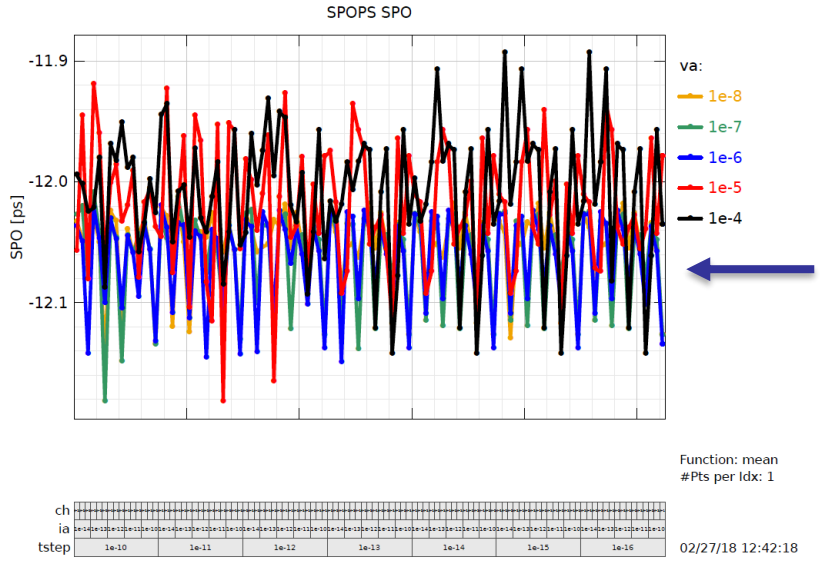
Time step outliers

Depends on many parameters – time step, charge tolerance, vabstol, iabstol

Must check (sweep) all combinations of simulation parameters to ensure results are modeling the actual circuit rather than simulator noise



Iabstol outliers

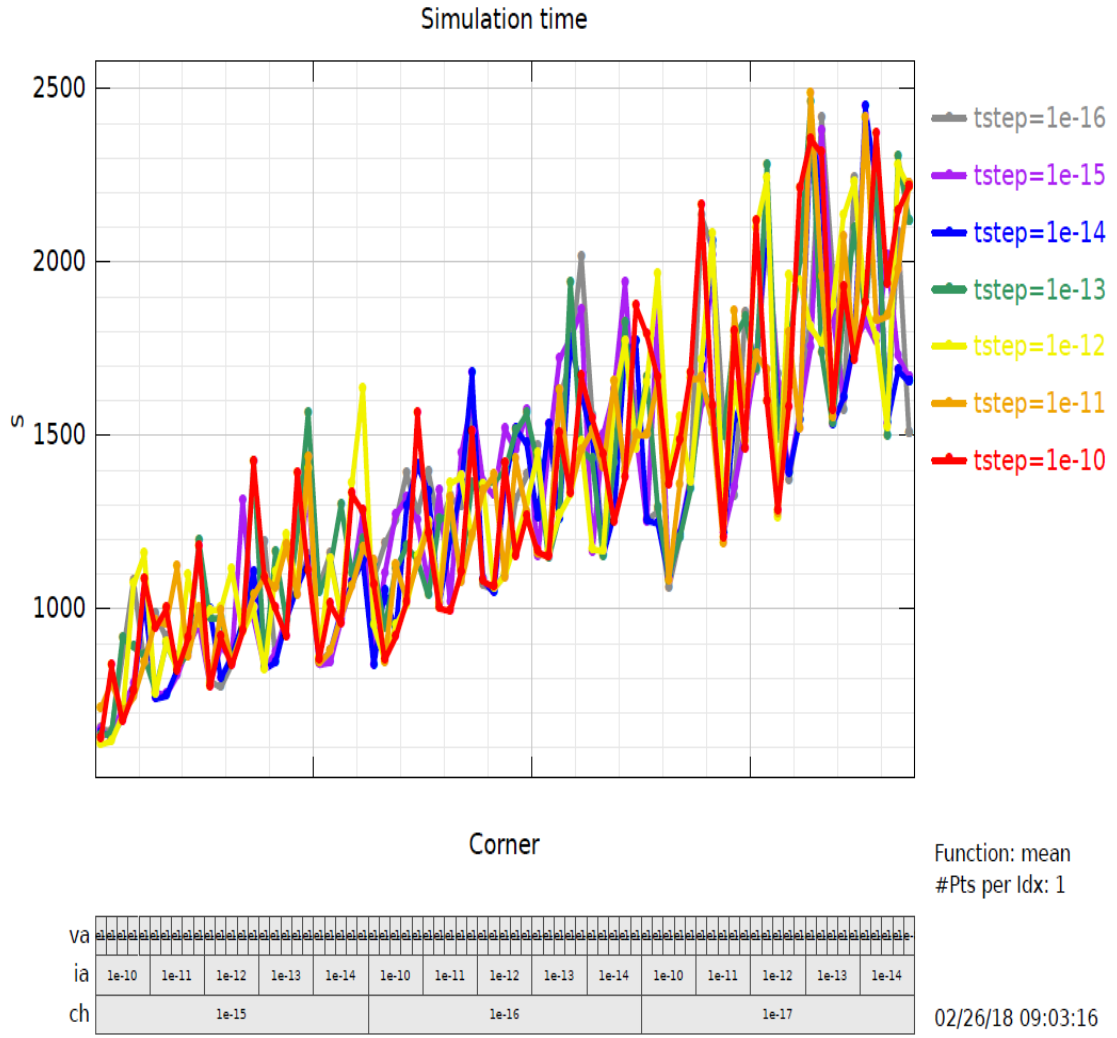


Valid simulation parameter combinations:

AFS defaults are okay for most circuits, but should always be checked!

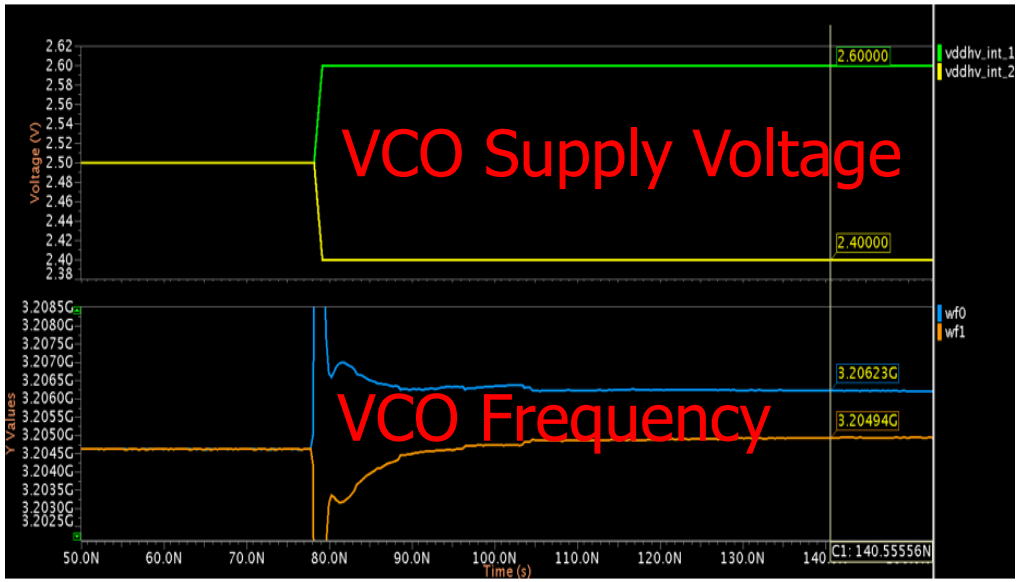
Charge Pump Simulation Time

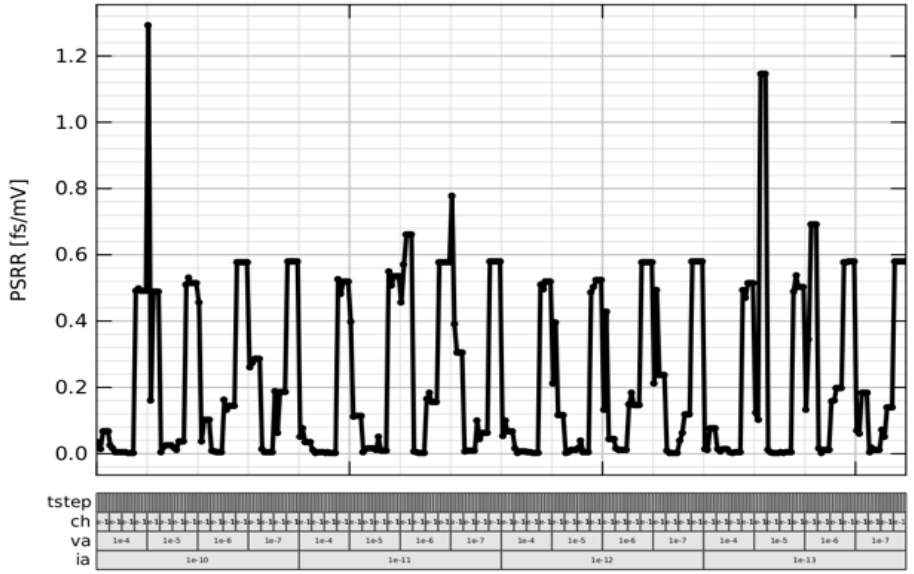
- Simulation time can be optimized by finding the largest charge tolerance that give accurate results
- Simulating with a tighter tolerance than needed provides no additional design insight, but can slow down simulations by 2X-3X
- For high performance ring oscillator PLLs, it was found that a charge tolerance of 1E-15C results in optimal accuracy/speed trade-off
- Vabstol, iabstol, and timestep were not dominant factors



VCO PSRR

VCO "PSRR"
= Change in Frequency ÷ Change in Voltage





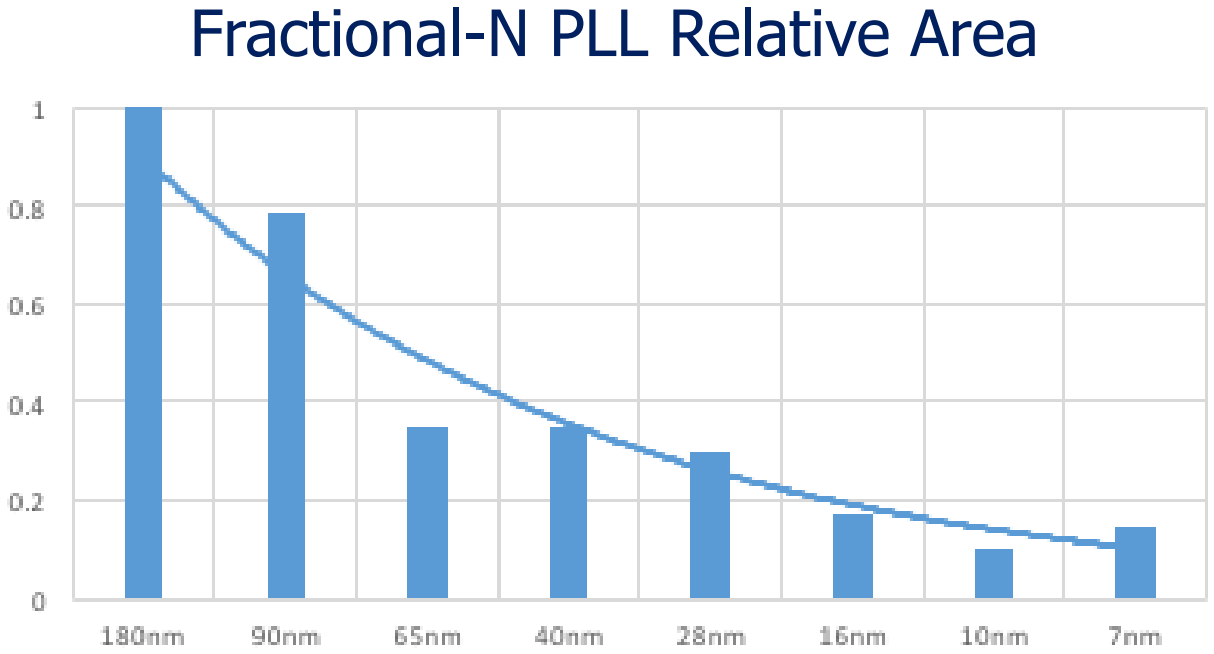
Result depends heavily on simulation parameters. Getting an accurate result is critical for predicting jitter

Typical Values (fs/mV):

Optimized 3.3V PLL	<1
Standard 1.8V PLL	<20
Core voltage PLL	<100

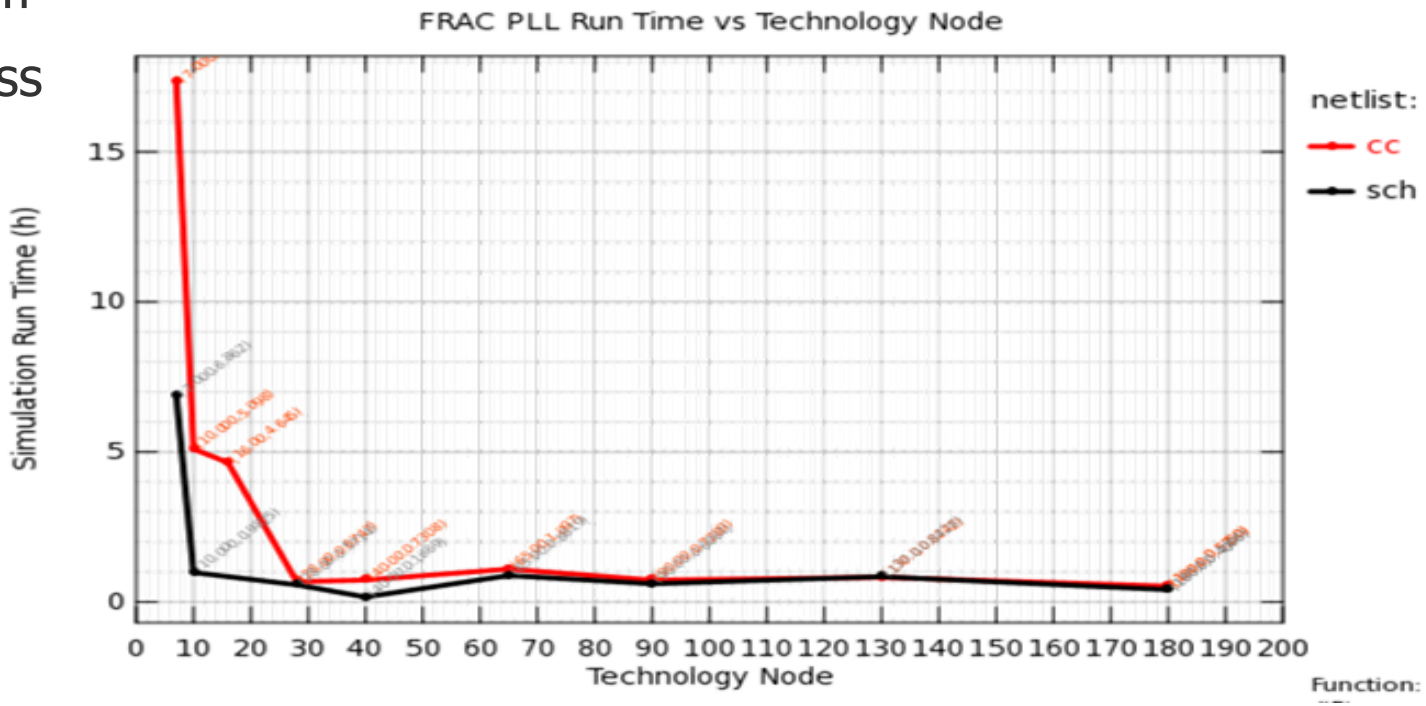
Analog Scaling – to 7nm

- There is some debate over whether analog "scales"
- Holding noise constant (kT/C), the area should scale with cap area – and does!
- Analog functions scale, but not as well as digital … from 180nm to 7nm:
  - Digital scaled ~661:1
  - Analog scaled ~10:1



Simulation speed vs. Process node

- Silicon Creations' fractional PLL has been ported to every process node from 180nm to beyond 7nm
- Simulated to lock to compare simulation time
- Planar process show minimal variation in time to lock from 180nm down to 28nm
- FinFET process → significant jump in simulation time and in memory usage



Schematic

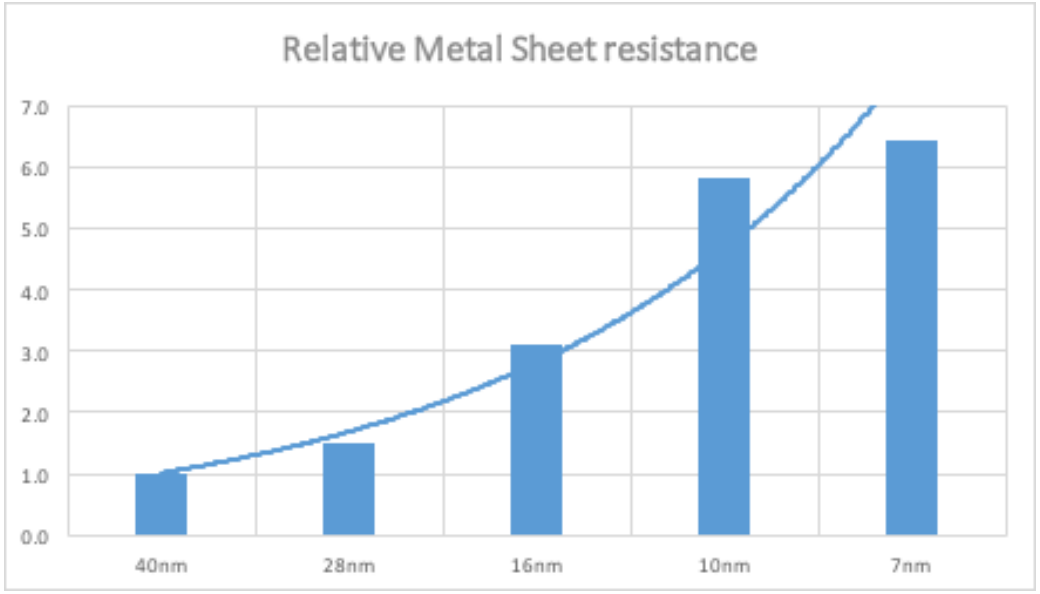
Node	HMS	Total_H	Total_M	Total_S
7	06:51:42	6.86	411.70	24702
10	00:58:57	0.98	58.95	3537
28	00:34:17	0.57	34.28	2057
40	00:10:01	0.17	10.02	601
65	00:52:55	0.88	52.92	3175
90	00:36:22	0.61	36.37	2182
130	00:50:34	0.84	50.57	3034
180	00:24:31	0.41	24.52	1471

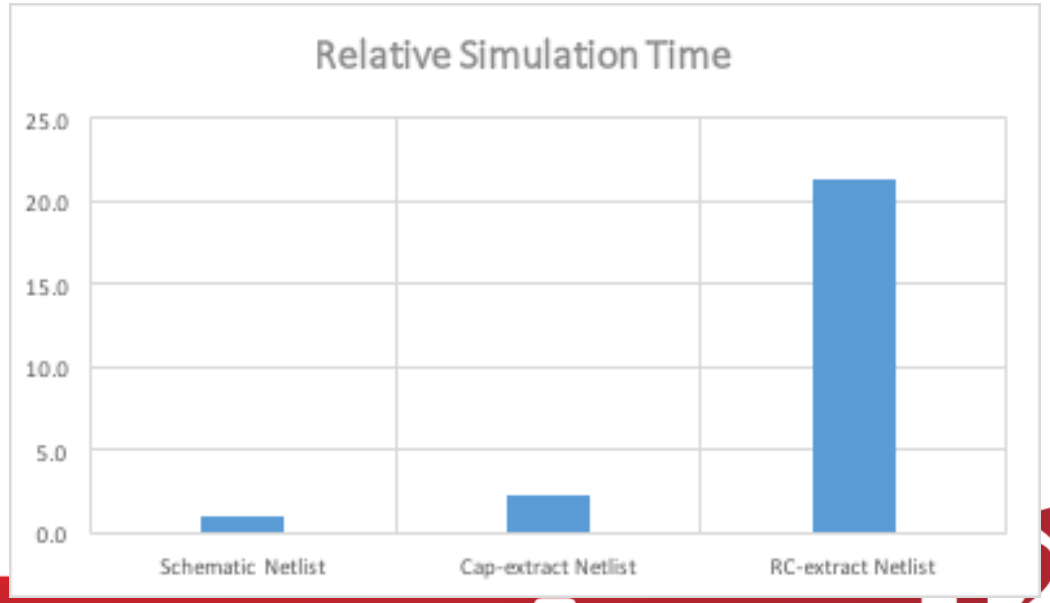
CC-Extracted

Node	HMS	Total_H	Total_M	Total_S
7	17:19:36	17.33	1039.60	62376
10	05:05:54	5.10	305.90	18354
16	04:38:43	4.65	278.72	16723
28	00:40:29	0.67	40.48	2429
40	00:43:51	0.73	43.85	2631
65	01:05:50	1.10	65.83	3950
90	00:43:44	0.73	43.73	2624
130	00:49:27	0.82	49.45	2967
180	00:31:30	0.53	31.50	1890

7nm Design Challenges – Simulation Time

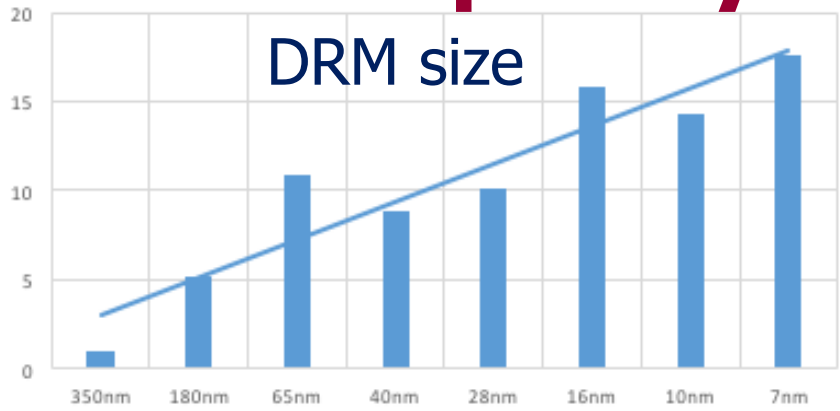
- In advanced processes, analog designs are becoming limited by wire performance
- Schematic sims are out, CC and RC extracted sims are needed (RC reduction can help)
- Translates to:
  - Longer development cycles
  - Need for more simulation licenses
  - Need for parallel simulation licenses
  - Higher development costs!

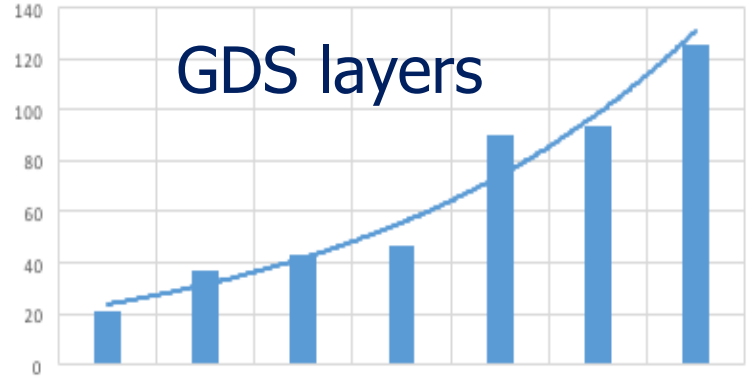


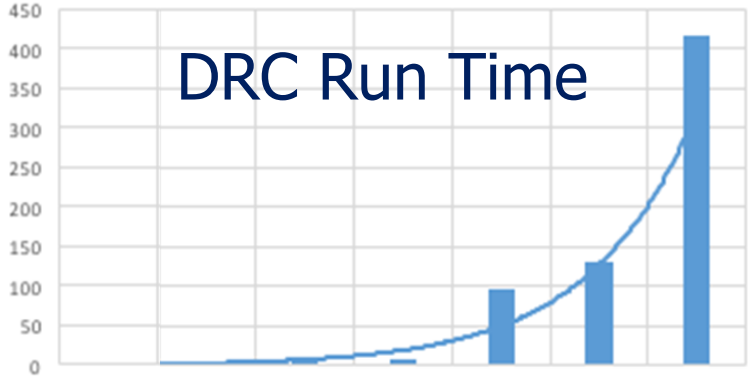


7nm Design Challenges – Process Complexity

- Relative DRM size
  - From 350nm to FinFET, the # DRM pages has increased drammatically
  - Correlates with an increase in process complexity
- Number of GDS layers
  - Increased 5x since 180nm
  - Measure of design and process complexity
- Relative DRC Run Time
  - Tighter more complex rules, more fill geometries
  - Run times compared to 28nm:
    - 16nm FinFET are ~10x longer
    - 7nm FinFET are ~50x longer

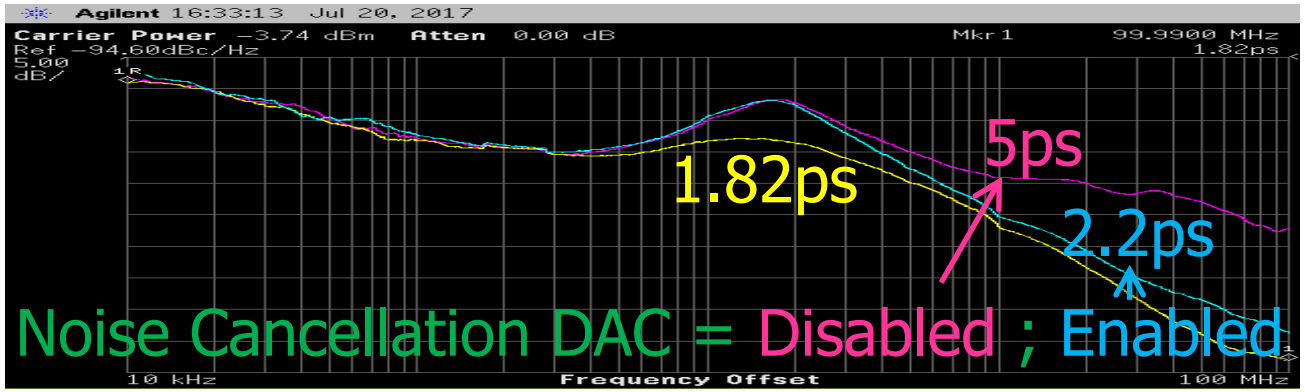


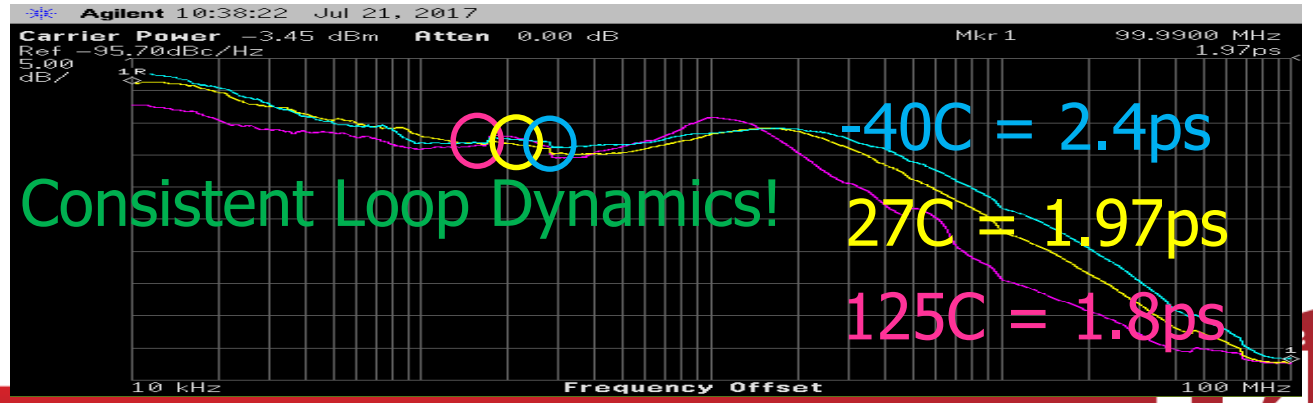




Fractional PLL Phase Noise

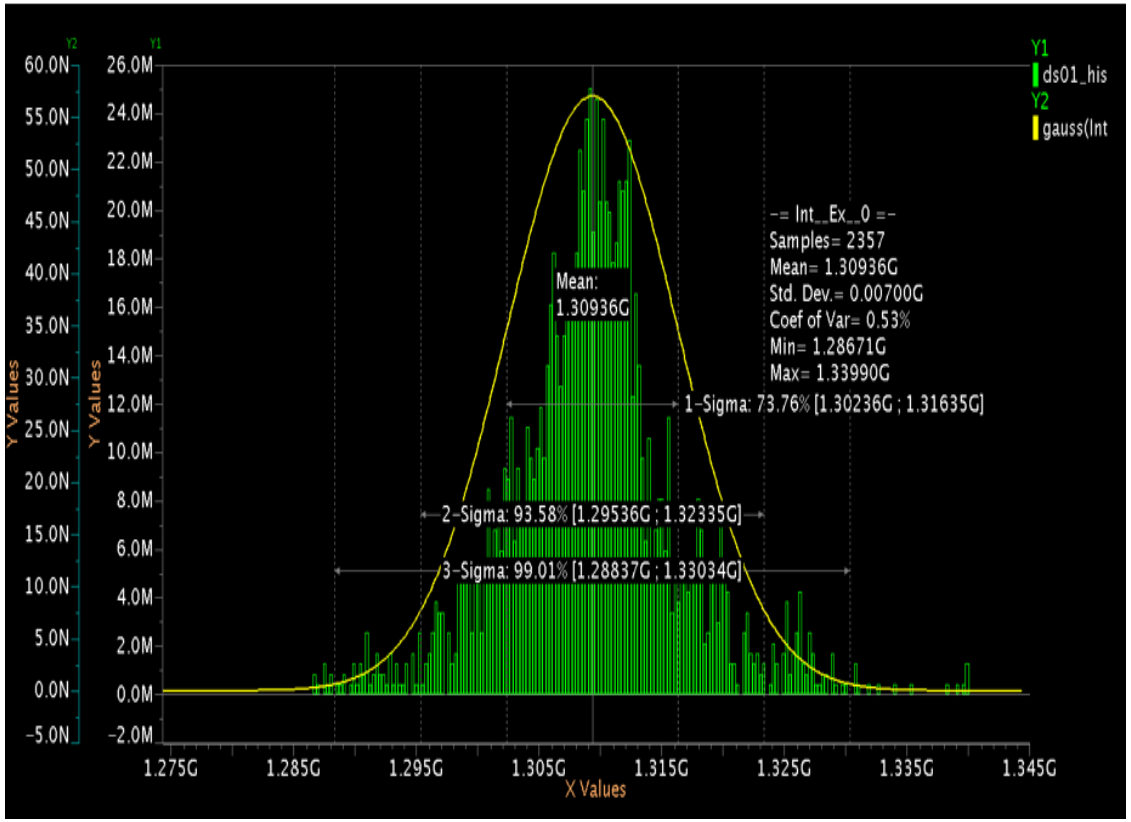
- Phase Noise vs. Process Corner
  - FastN/FastP
  - TypN/TypP
  - SlowN/SlowP
- Phase Noise vs. Operating Mode
  - Fractional Mode, Noise cancellation DISABLED
  - Fractional Mode with Noise Cancellation
  - Integer Mode
- Phase Noise vs. Temperature





Transient Noise Analysis

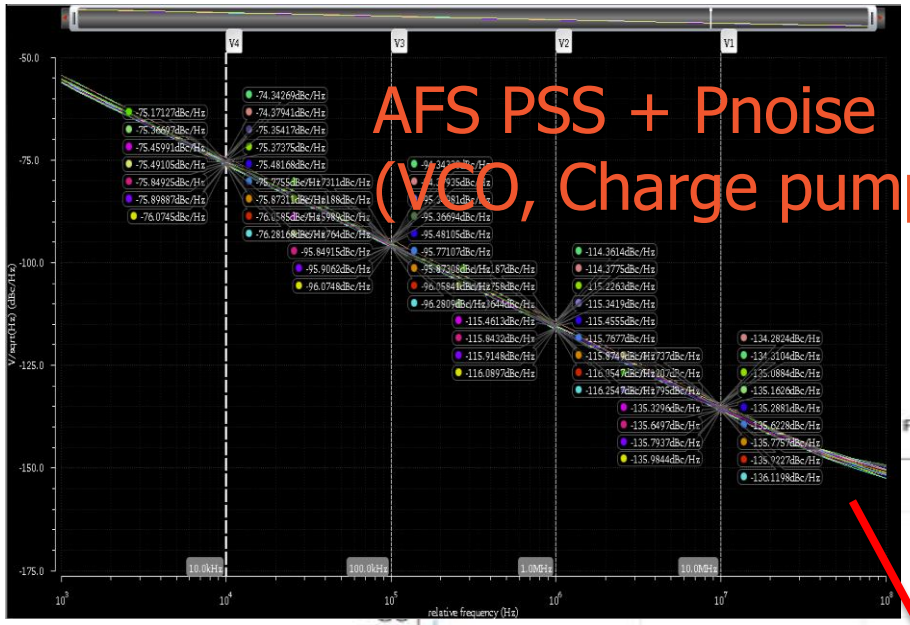
- Transient noise simulations were performed to correlate with the PSS+Pnoise overlays
- RMS jitter results deviated significantly from measured results
  - Run time was 2µs after lock
- For 32kHz PLL, it is not possible to simulate for the 10s of ms that would be required to get an accurate result

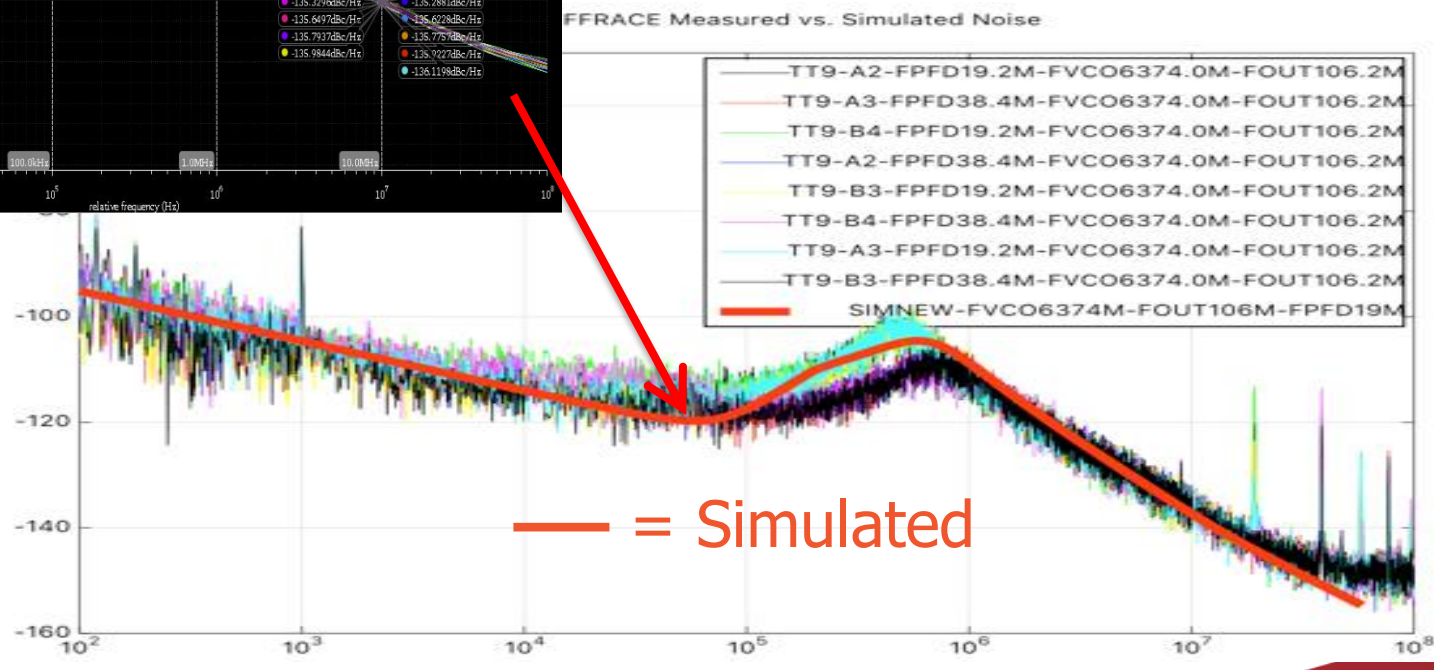


PLL Type	Trannoise	Simulated Pnoise	Measured Pnoise
Standard Dual-Voltage Fractional PLL	0.56	0.84	1.20
Jitter-Optimized Dual-Voltage Fractional PLL	4.08	1.20	0.99
Area Optimized Core-Voltage Integer PLL	4.28	1.68	2.34
32kHz Power-Optimized Dual-Voltage Integer PLL	11.61	619.00	336.00

Fractional PLL Simulation vs. Measurement

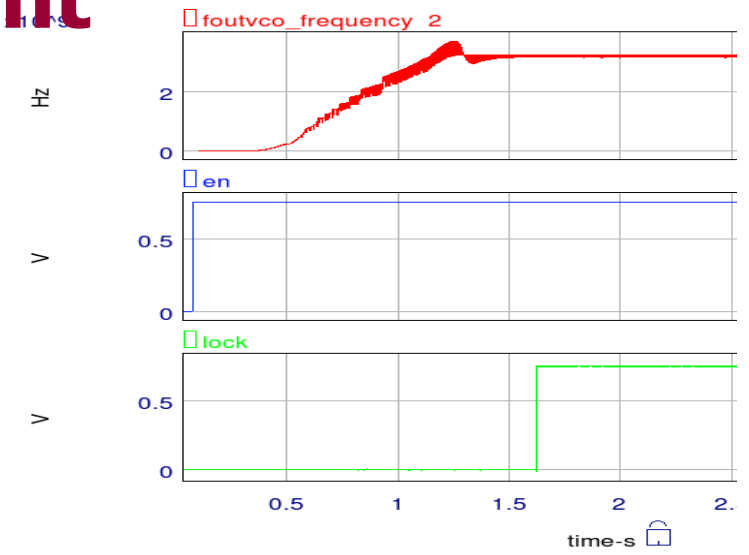
Excellent correspondence between AFS derived phase noise and measured performance

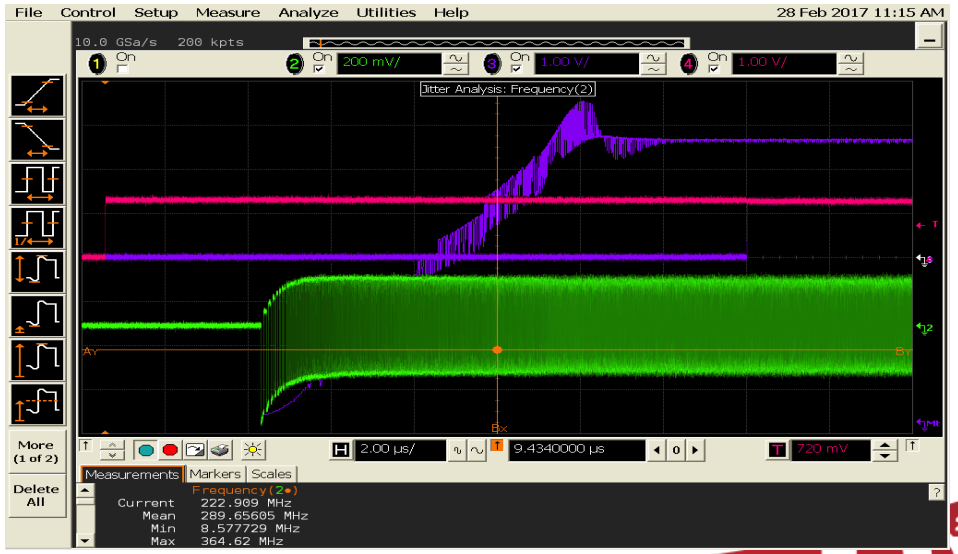




Core Voltage, Area Optimized PLL Locking Simulation vs. Measurement

- Lowest area PLL for digital clocking – 0.009mm^2
- Total power under 200µW
- Excellent correspondence between AFS transient simulation (frequency vs. time) and measured result



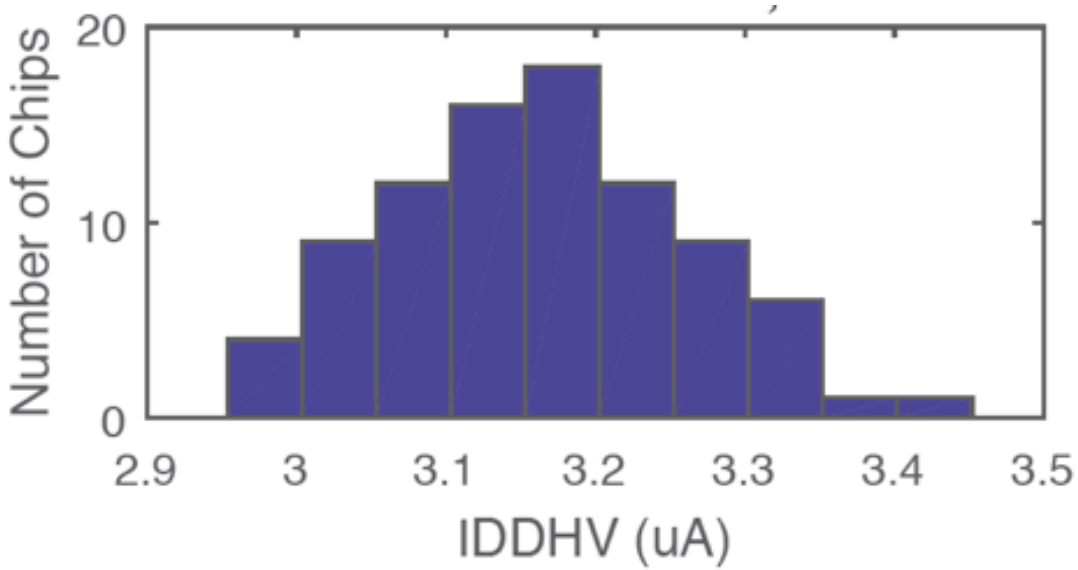


7nm IoT PLL Current Consumption

- **Simulation**
  - Mean=3.02uA
  - Stddev=1.5%

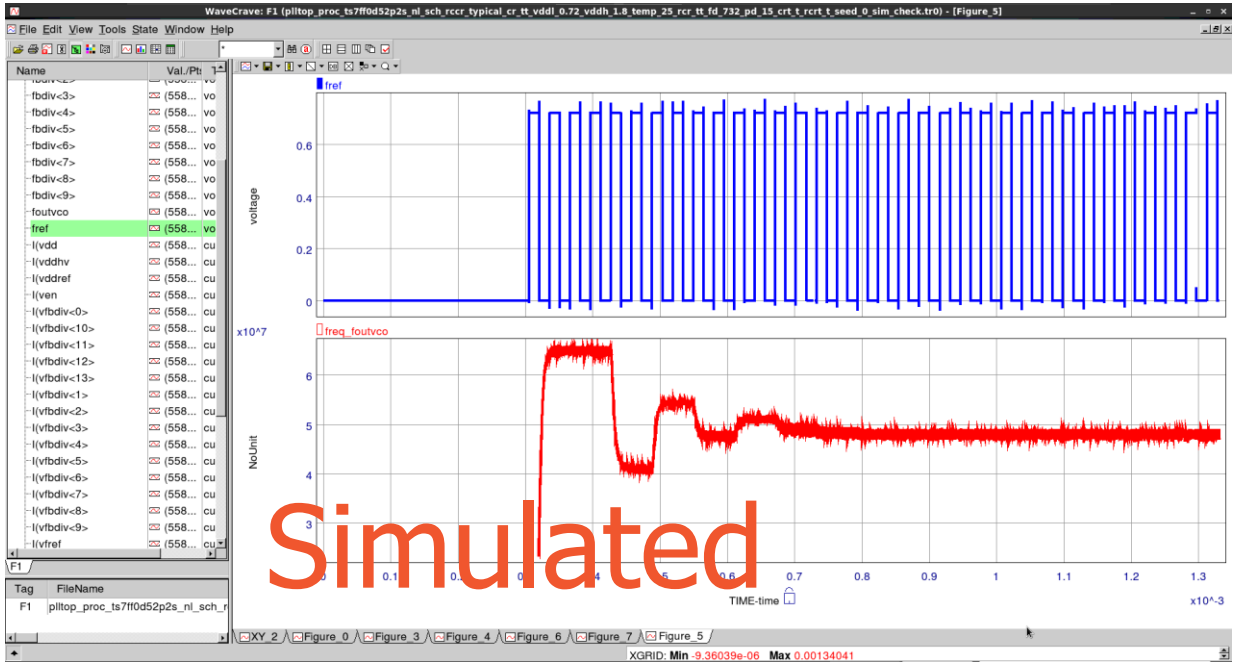
- **Measurement**
  - Mean=3.15uA
  - Stddev=1.6%

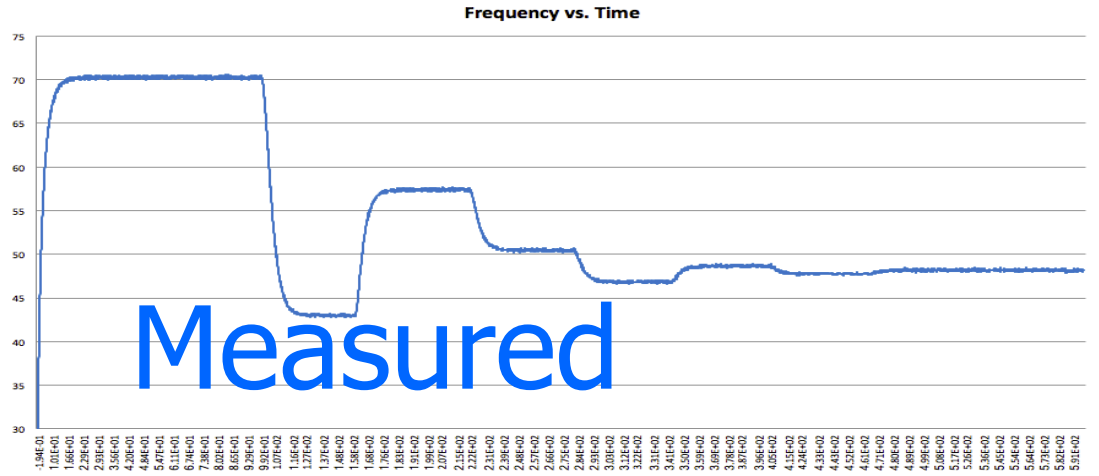
Measured Current Distribution



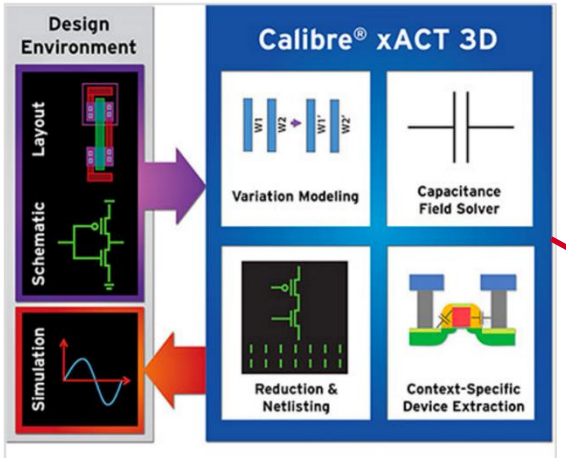
IoT PLL Fast Locking

- AFS transient simulations accurately predict locking behavior
- 32kHz locking simulations must run for >1ms, so require a fast simulator AND fast locking PLL!



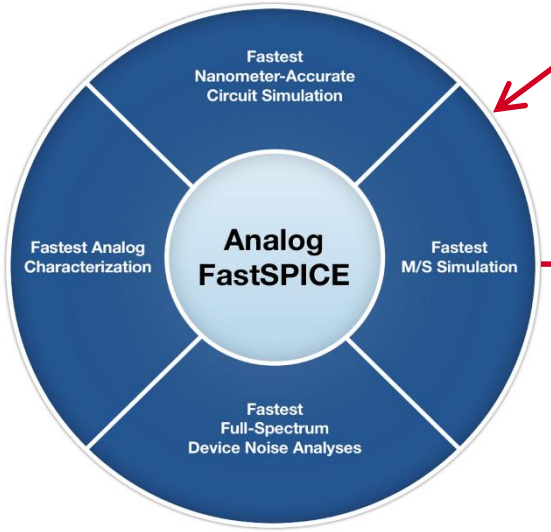


EM/IR/EOS Flow

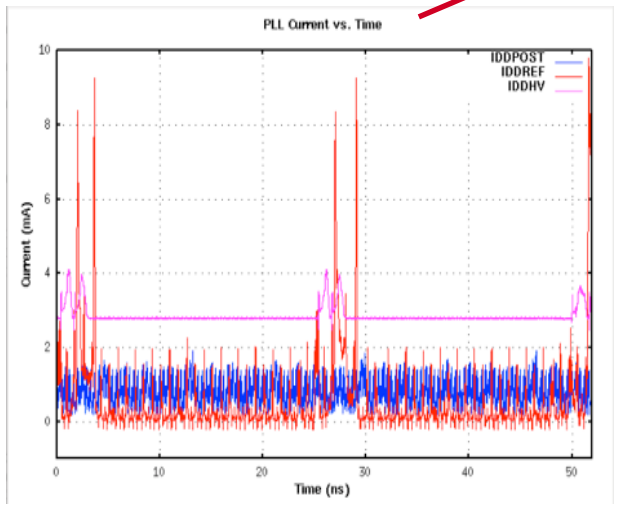


DSPF Netlist generated by XACT-3D

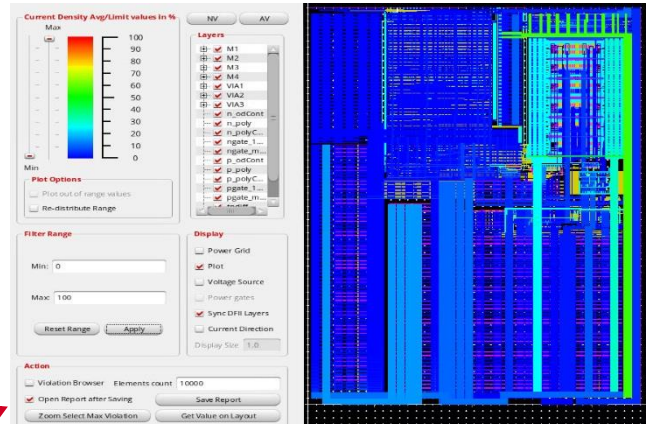
```
*|DSPF  1.5
*|DESIGN        PLLTS7FFFRACG
*|DATE  "Wed Jul 12 2017"
*|VENDOR        "Mentor Graphics Corporation"
*|PROGRAM       "xACT"
*|VERSION       "v2017.1_25.22"
Cc_2175598 VTUNEI:131089 dni<1>:47 0.0106871f
Cc_2175599 VTUNEI:130549 dni<1>:48 0.0106973f
R2195052 X103/X5150/X61_noxref:g VTUNEI:956927 28.2878 $w=0.135 $l=0.139
+ $layer=pgate_18_pode3t $X=158.8455 $Y=30.9000 $X2=158.8455 $Y2=31.0390
R2195053 X103/X5150/X61_noxref:g VTUNEI:957340 28.2878 $w=0.135 $l=0.139
+ $layer=pgate_18_pode3t $X=158.8455 $Y=30.9000 $X2=158.8455 $Y2=30.7610
```



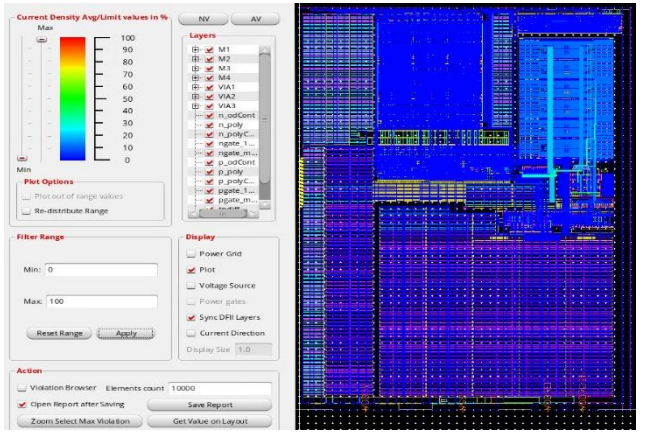
Closed-loop, RC-extracted Simulation



Accurate Device Currents

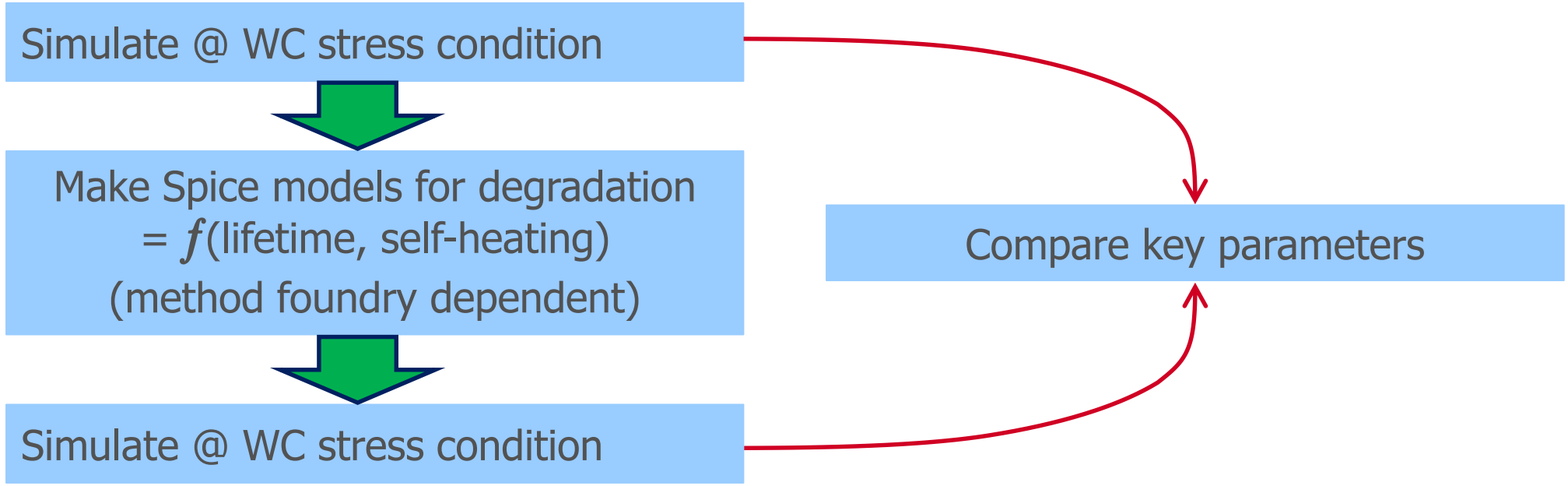


Power grid current density



Signal grid current density

Aging Simulation Flow



7nm IoT PLL (WC stress = SS corner, 10 years @ 125°C, Vdd's +10%)	**Before**	**After**	**Δ**
Current consumption	41.8uA	42.9uA	2.6%
FOUTVCO frequency (open loop)	99.3MHz	94.6MHz	-4.7%
FOUTVCO Duty Cycle	49.4%	49.4%	-0.08%

Outline

- Silicon Creations introduction
- Product overview
- Key PLL Specifications and Applications
- Introduction to PLL architecture and core building blocks
- Simulation benchmarking and Silicon Results
- **Summary**

Summary

- Silicon Creations provides PLLs, interfaces like LVDS and SerDes to 25Gbps
- Market leader in PLLs – already in production in 7nm, well underway in 5nm
- Designing in FinFet brings many challenges including simulation complexity and runtime; need to pay close attention to parasitics, proximity and matching, and balance accuracy and design time
- 7nm is significantly more complex than 16nm/12nm, but no new techniques are needed; the same PLL circuit topology has worked from 180nm to 7nm
- Good simulation-silicon correlations are possible with our Mentor-based design flow

Useful References

- www.siliconcr.com
- Silicon Labs AN279 – Estimating Period Jitter from Phase Noise
- Silicon Labs AN256 – Integrated Phase Noise
- Silicon Labs AN687 – A Primer on Jitter, Jitter Measurement, and Phase Locked Loops
- Analog Devices MT-008 – Converting Oscillator Phase Noise to Time Jitter
- http://www.delroy.com/PLL_dir/tutorial/PLL_tutorial_slides.pdf
- http://www.designers-guide.org/
- https://www.jitterlabs.com/support/training/online-classes

Please complete a session survey in the U2U Conference App.

USER2USER