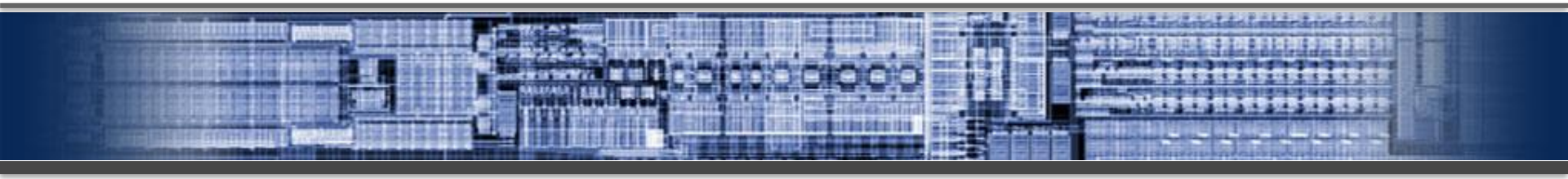


Flexible clocking solutions in advanced processes from 180nm to 5nm

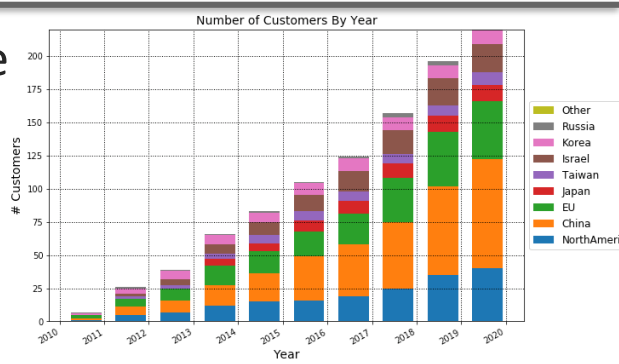
Andrew Cole & Randy Caplan

Outline

- Silicon Creations introduction
- Kinds of jitter and a DAC inside a PLL
- Flexible clocking solutions with FRAC PLLs
- Other PLLs and clocks
- Summary

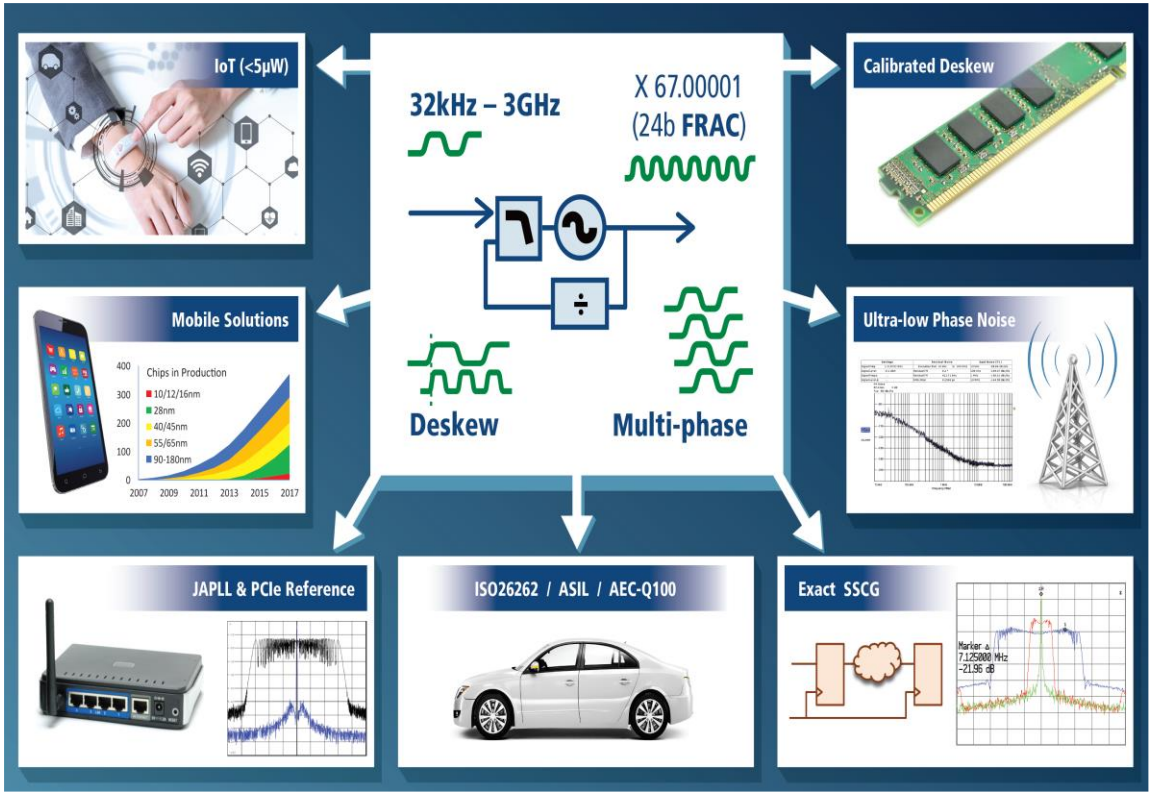
Silicon Creations Overview

- IP provider of PLLs, Oscillators, and High-speed Interface
- Founded 2006 – self-funded, profitable, and growing
- Design offices in Atlanta, USA and Krakow, Poland
- High quality development, award winning support
- >220 customers (>25 in Israel)
- Mass production from
  7nm to 180nm,
  5nm silicon proven
- IP support in all major foundries



PLLs from Silicon Creations

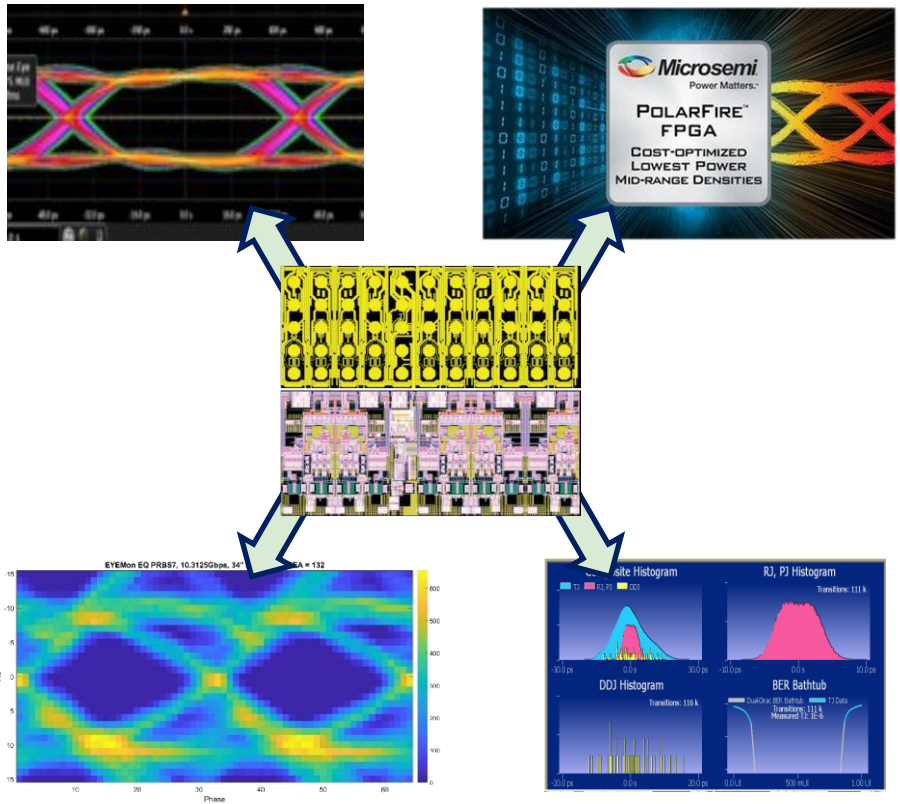
- Highest volume analog IPs … robust design and good QA are essential. E.g.
  - 28nm FRAC PLL >135 MP tapeouts, >1.5M wafers, >4B PLLs
  - 16nm FRAC PLL >50 MP tapeouts, >1M wafers, >3B PLLs
- PLL products include general purpose, fractional, low jitter AFE, µW IoT, Automotive



SerDes from Silicon Creations

- Robust and proven from 12nm to 180nm and from <100Mbps to >25Gbps
- Multiprotocol in 12nm, 16nm, 40nm
- Targeted protocols including

  SGMII, XAUI, RapidIO,
  V-by-1 HS/US, DP, FPDLink,
  OIF-CEI, JESD204, CPRI,
  PCIe1-5, 10G-KR, …



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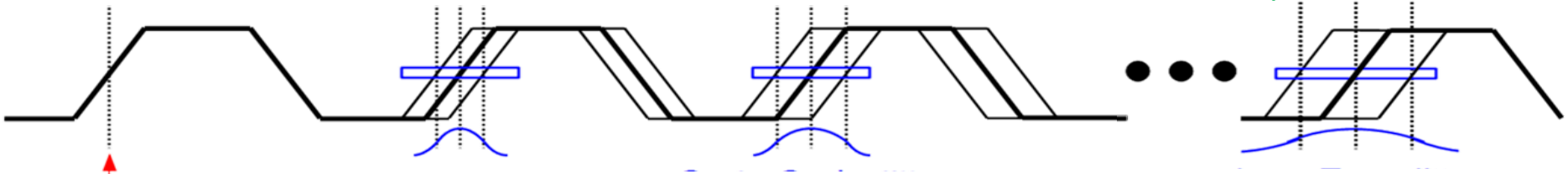
Types of Jitter



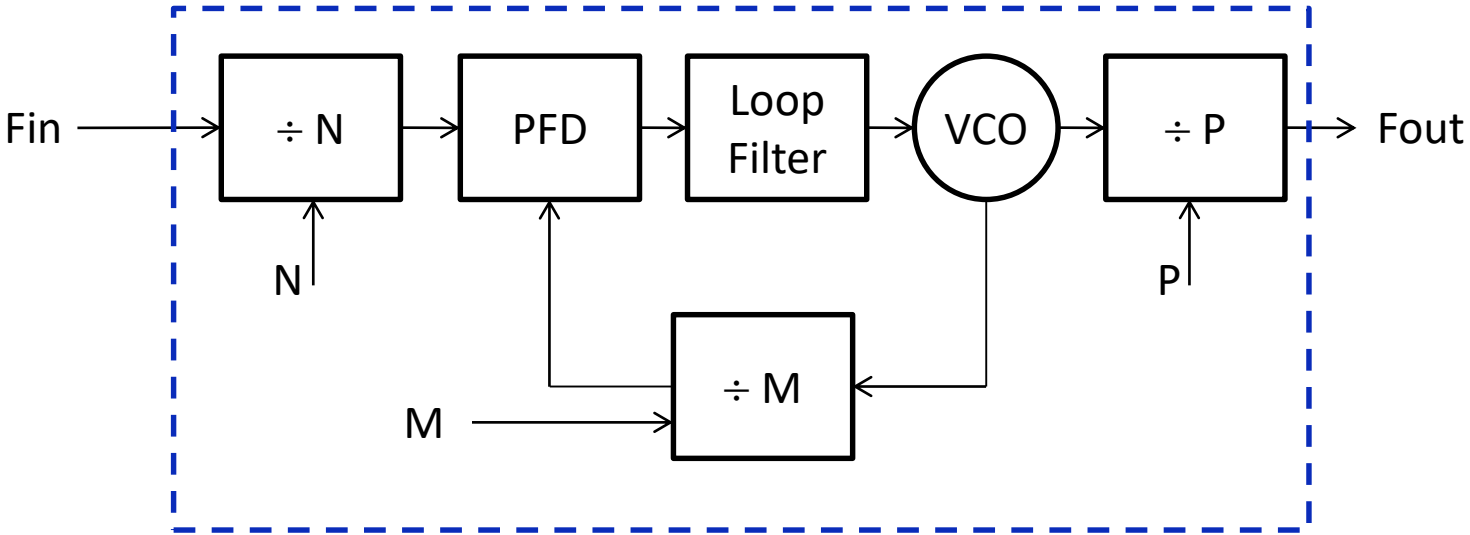
Short term jitter – determined by VCO

Important for digital timing ("STA")

Determined by PLL closed loop

Important for ADC/DAC and SerDes

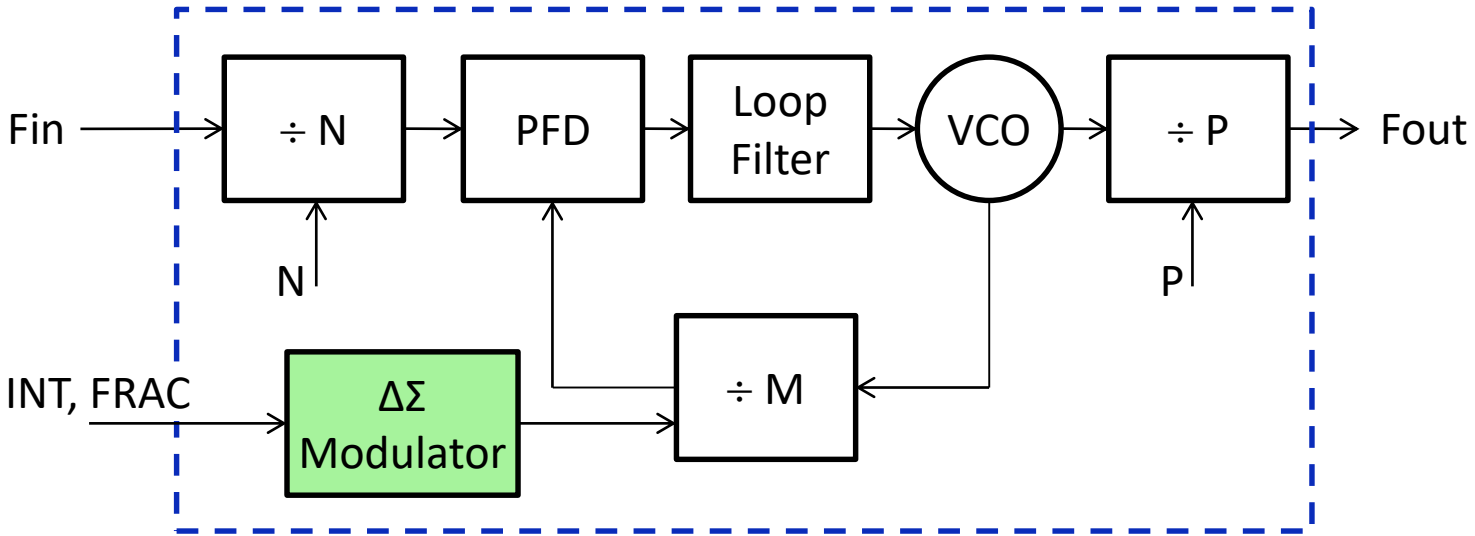
Conventional Integer PLL



$$\text{Fout} = \frac{\text{Fin}}{\text{N}} \times \frac{\text{M}}{\text{P}} \qquad \frac{\text{Fout\_step}}{\text{Fout}} \approx \frac{1}{\text{M}}$$

With typical $\text{M} > 50$, LSB change in Fout $< 2\% = 20{,}000\text{ppm}$

Fractional-N PLL



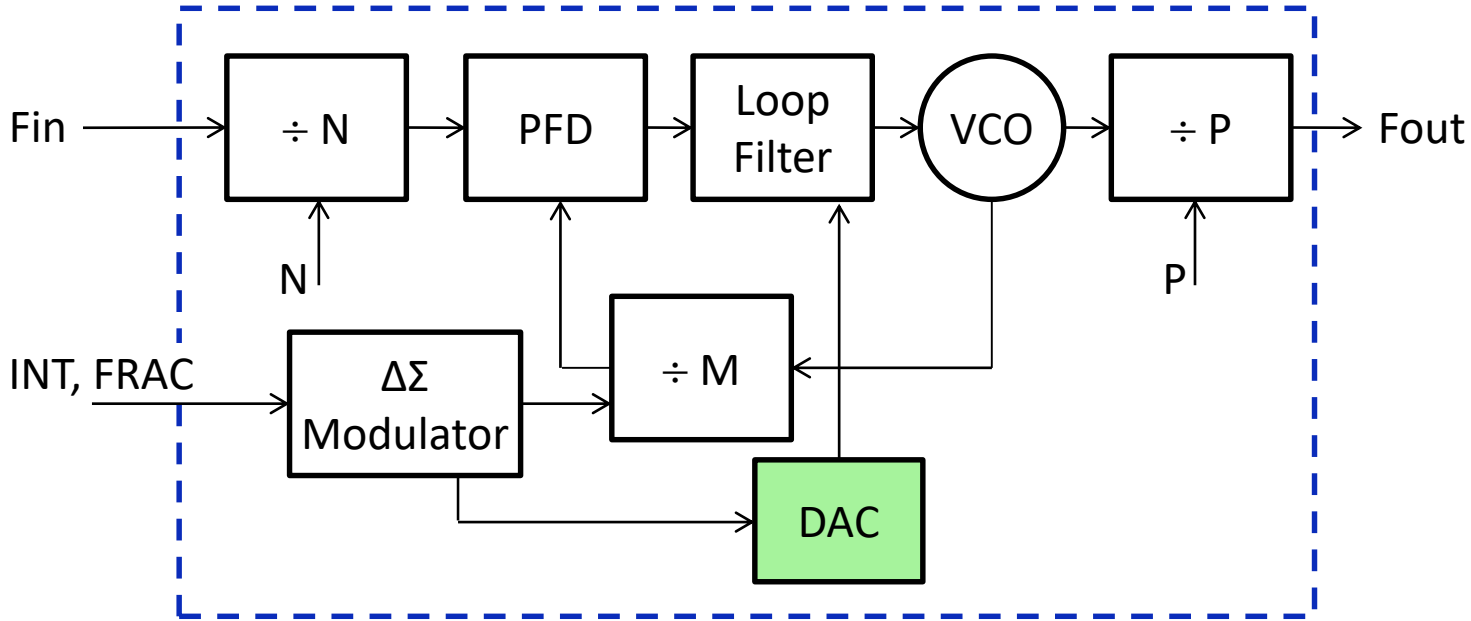
$$M\_avg = INT + \frac{FRAC}{2^X} \qquad Fout = \frac{Fin}{N} \times \frac{M\_avg}{P} \qquad \frac{Fout\_step}{Fout} \approx \frac{1}{M \times 2^X}$$

With $x = 24$ (bits), typical $M > 20$, LSB change in Fout < 0.003ppm

E.g. Average FBDIV of 10.25

"Order"	Values	Sequence
1	10+ 0, 1	0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1  ☺ Simple ☹ Repeats at ¼ Fin … "spurs" in Fout
3 ✓	10+ -2, -1, 0, 1, 2, 3	1 0 1 -2 3 -2 2 0 0 2 -1 0 1 0 0 -2 1 0 0 1  ☺ Tones (spurs) much reduced ☹ More complex

DAC to Fix Fractional Jitter

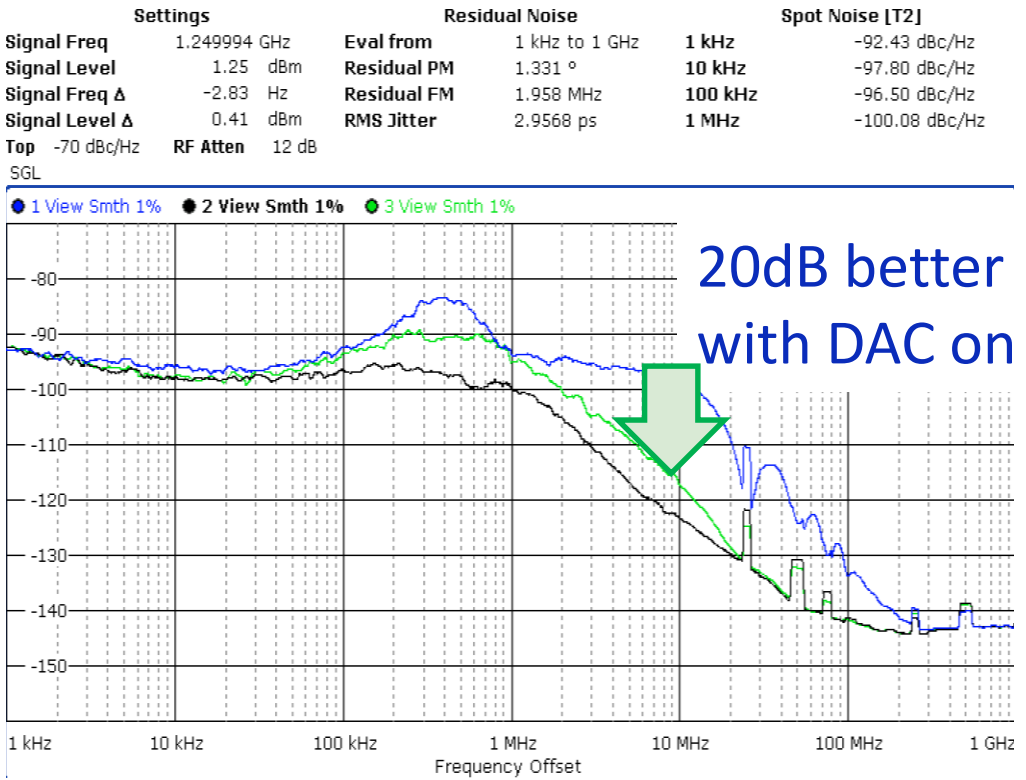


Feed inverse of impulse errors forward to loop filter. DAC re-uses existing transistors and current, so adds almost no area, and almost no power.

DAC Performance Measured

Phase noise with and without DAC. Performance is improved dramatically.

- ✓ Flexible: Any output frequency with any Xtal
- ✓ Good PPA: Use FRAC PLL to make a low jitter clock e.g. SRIS clock for PCIe



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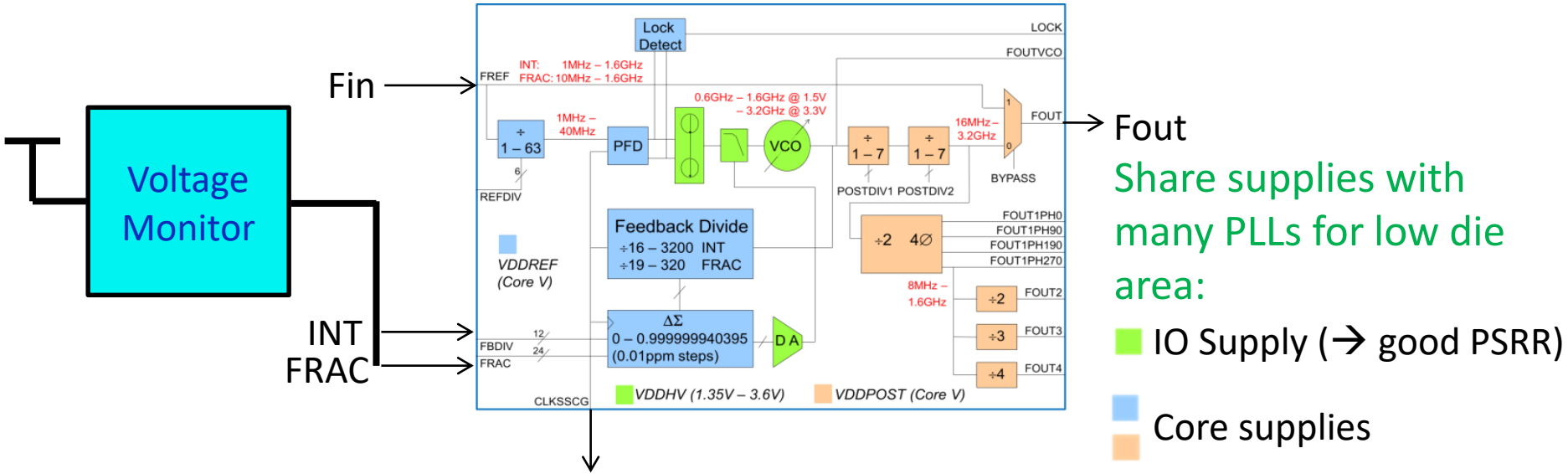
DFS & Supply Sharing



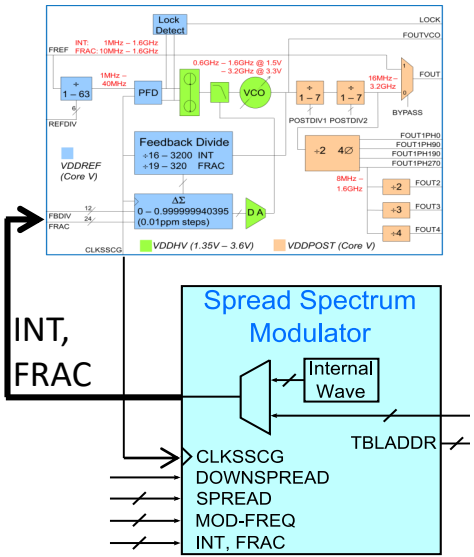
Share supplies with many PLLs for low die area:

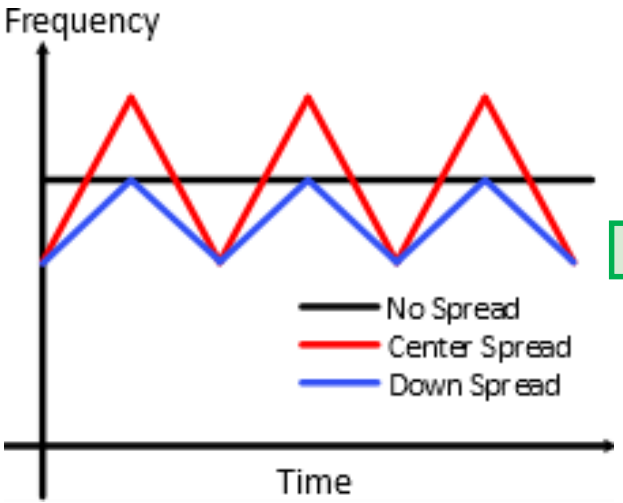
- IO Supply (→ good PSRR)
- Core supplies

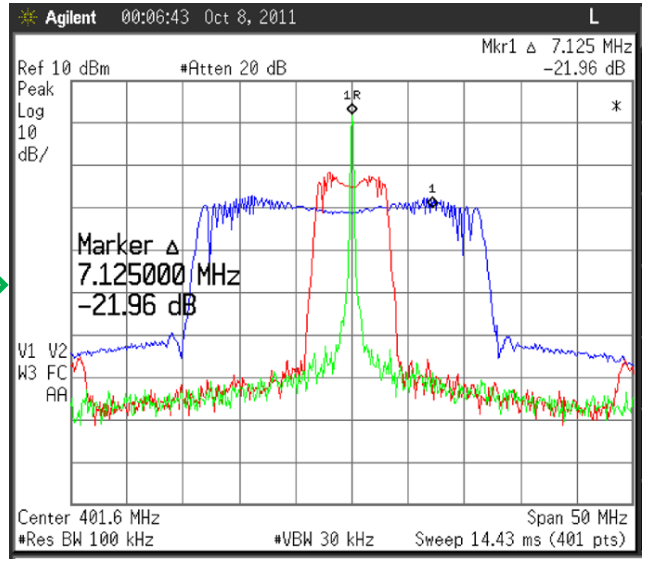
FB Clock output – allows new INT, FRAC on every divided Fin edge. PLL will move predictably to new programmed frequency without losing LOCK for Dynamic Frequency Scaling (DFS).

Exact Spread Spectrum

Digital modulator continuously changes the target frequency for exact spread spectrum shape & modulation frequency. Soft IP (RTL), 4k gates

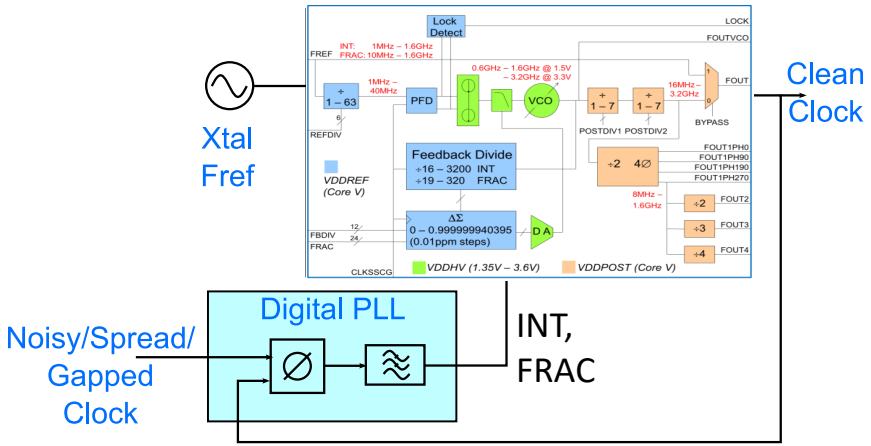


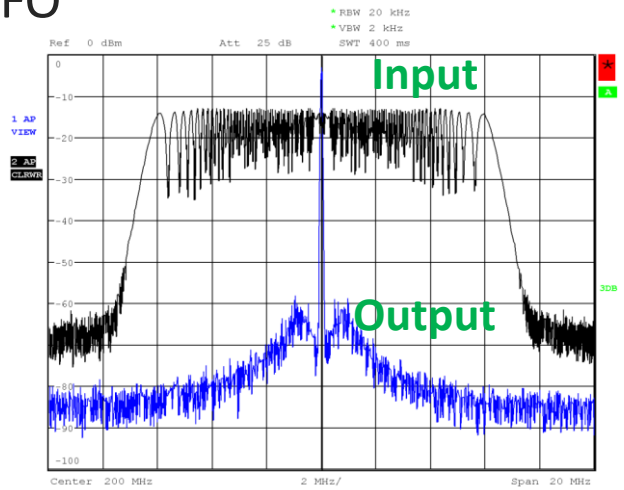




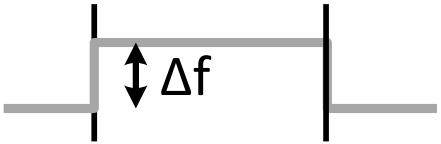
Jitter Cleaner PLL

- Digital Filter (RTL ≈19k gates) sets multiplier for fixed clock for FRAC PLL
- Integrated LTJ <1ps and Bandwidth <1Hz possible … replaces $8 to $30 external chip
- Cleans jitter in noisy recovered clock for Sync-E or Optical Networking; Generates average of spread spectrum input for FIFO



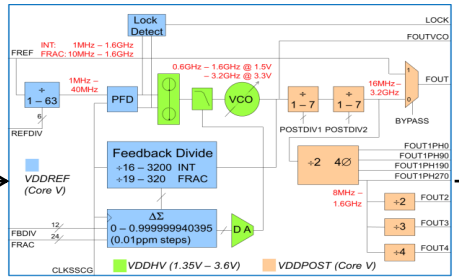


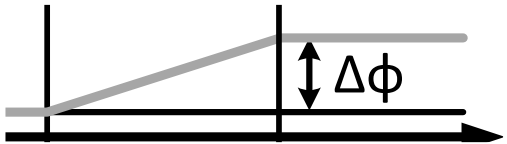
Exact Control of Output Phase



Frequency
Δf, Δtime

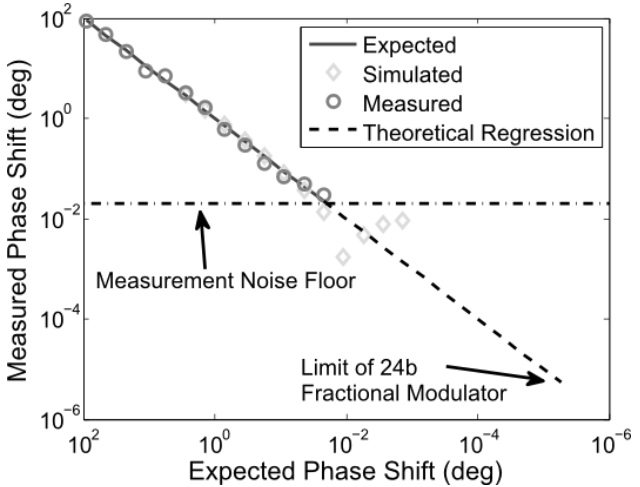
RTL





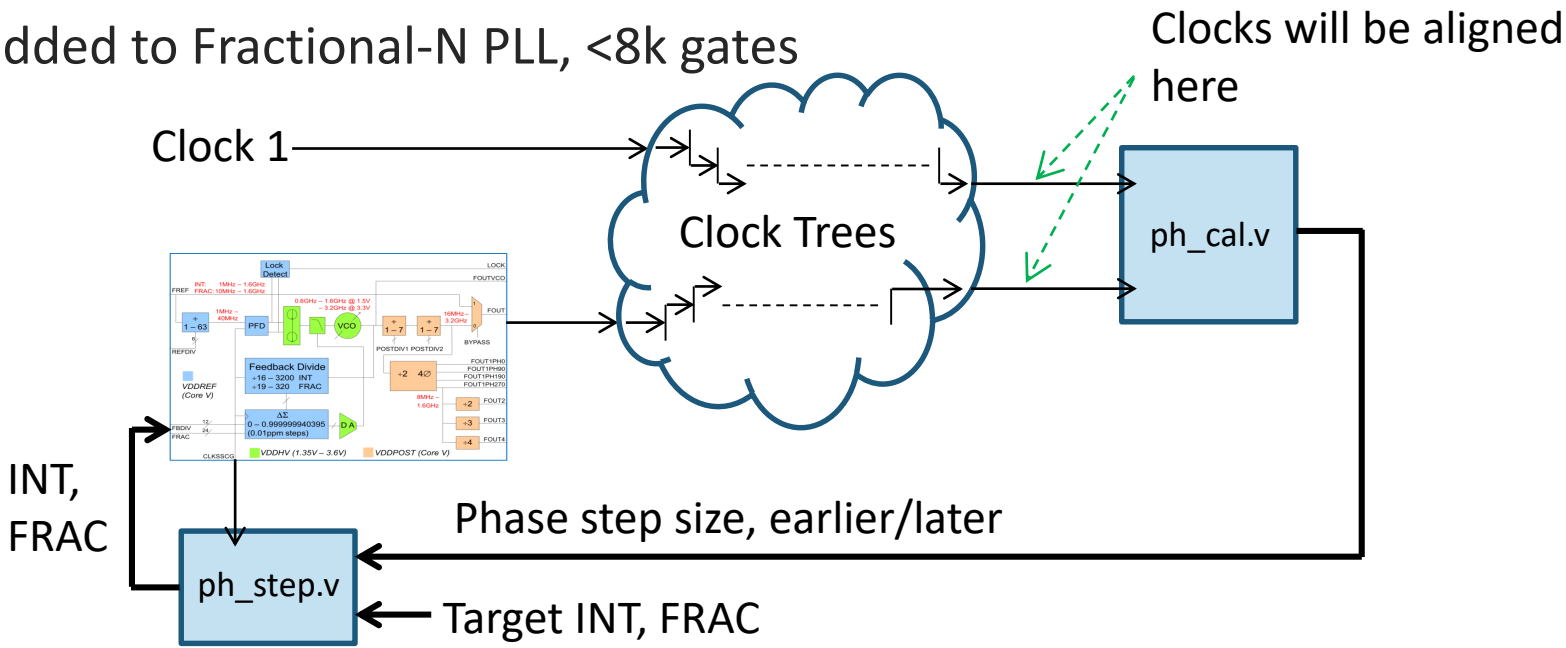
Precise Output
Phase Step

"Microdegree frequency and phase difference control using Fractional-N PLL synthesizers",
B. Gray, et. al., Microwave Symposium Digest 2012

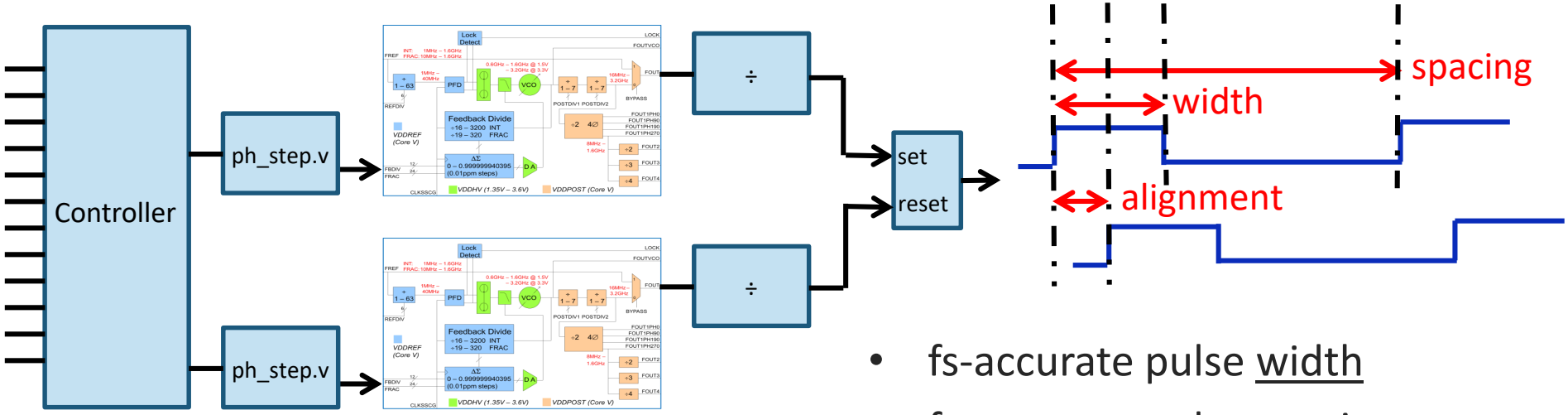


Anywhere Aligner

- Align two clocks anywhere in a chip by checking alignment and asking FRAC PLL to step phase in/out until aligned
- RTL added to Fractional-N PLL, <8k gates

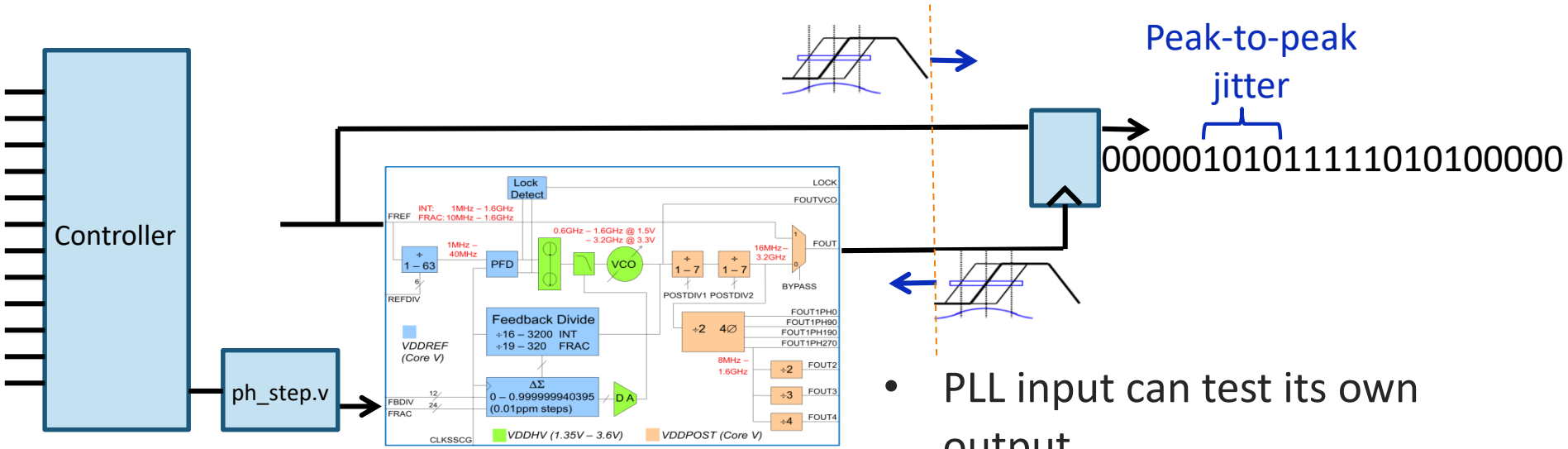


fs-Accurate Pulse Generator



- fs-accurate pulse width
- fs-accurate pulse spacing
- fs-accurate alignment between multiple channels

PLL Self-Test



- PLL input can test its own output
  - No external clock or 2nd PLL needed
- Production test screening

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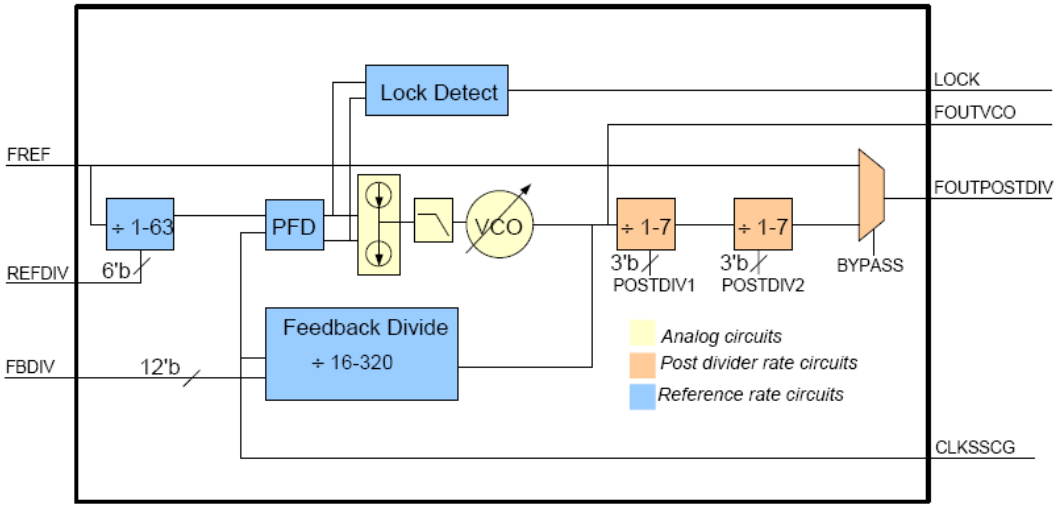
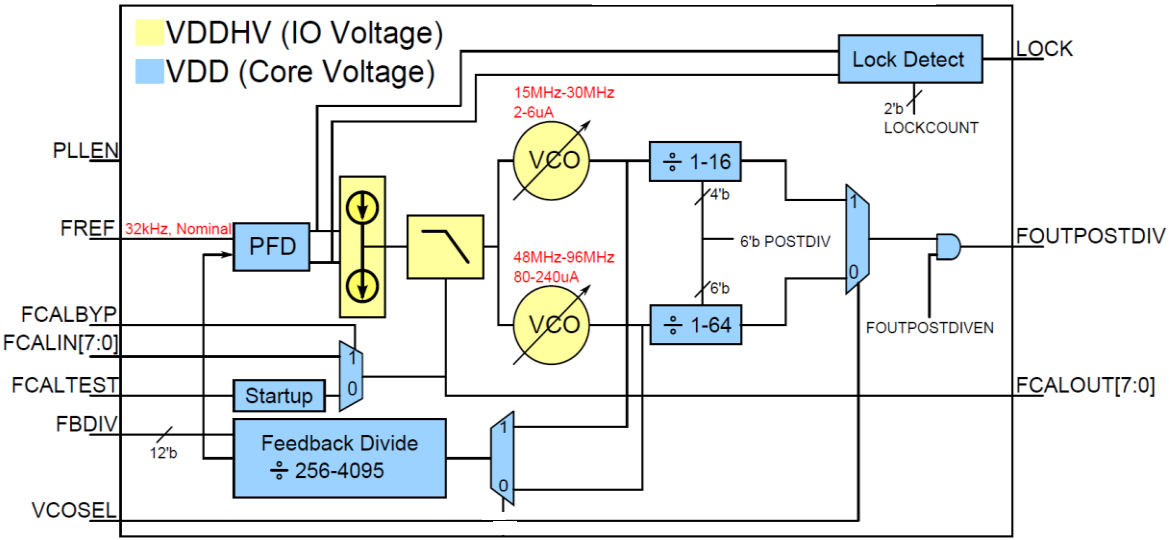
Low-Area PLLs

- Core voltage only, integer only … for digital core clocking
- Below 0.01mm^2 in advanced processes
- Very easy to integrate and low power



IoT PLL

- PLL power as low as **5µW** for whole PLL
- Uses an RTC (32.68kHz) reference – ultra-low power
- Fast starting – ±2% of freq. Cold in <1.2ms (40 cycles); Warm < 100us
- <0.12mm^2 in 40nm and below, with no external components

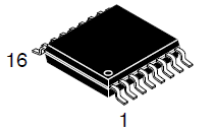


Low-jitter Ring PLL for PCIe4/5

ON Semiconductor®

NB3N51032

3.3 V, Crystal to 25 MHz, 100 MHz, 125 MHz and 200 MHz Dual HCSL/LVDS Clock Generator



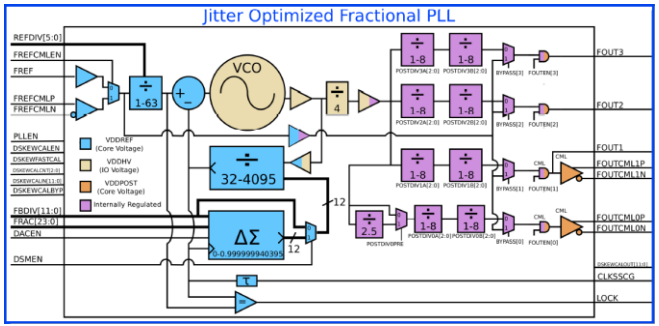
- Uses 25MHz external crystal resonator
- LVDS + HCSL output
- PCIe Gen 1, Gen 2, Gen 3, Gen 4 Compliant
- Typical power = 100mA from 3.3V = 330mW
  Add power for LVDS receiver in your chip

Digi-Key ELECTRONICS

Price Break	Unit Price
2,500	$1.80880

Silicon Creations

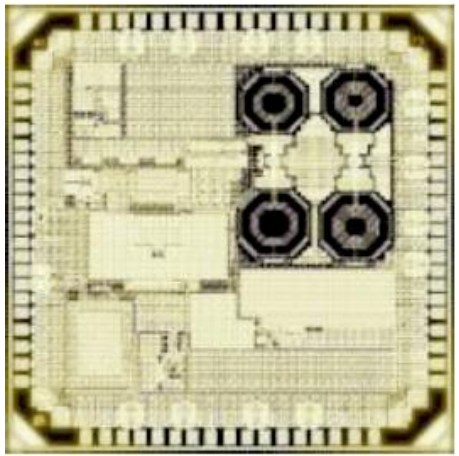
Low Jitter FRAC PLL

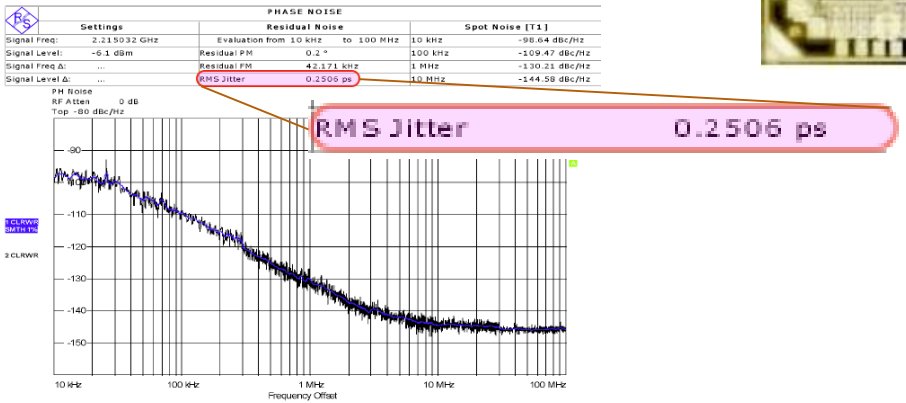


- Uses ≥19.2MHz Crystal clock from on-chip Xtal pad & external crystal resonator
- PCIe Gen 1-5 compliant including SRIS
- Typical power from 1.8V + coreV = 43mW
- LVDS receiver not needed
- <0.14mm^2 die area, 28nm to 5nm

Sub-ps LC PLLs

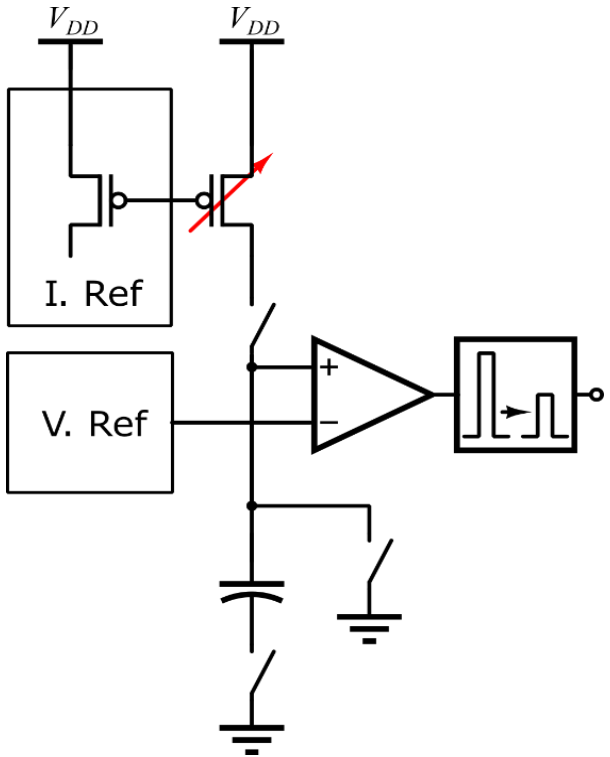
- Wideband integrated jitter as low as **250fs** from common crystal reference
- Fractional operation
  - All fractional mode techniques can be applied





Free-running Oscillators

- No external components
- Applications – watchdog timer, logic clock for ultra-low power mode (“IoT”)



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Summary

- Silicon Creations has been providing reliable, high performance clocking and SerDes solutions since 2006
- Our Fractional-N PLL is production proven with the highest volumes of any mixed signal IP
- Provides very flexible solutions to complex problems with low risk while reducing system BOM
- Optimized PLLs using the same core topology can use microwatts of power for IoT, negligible silicon area for digital chips or replace expensive discrete chips for SerDes clocks