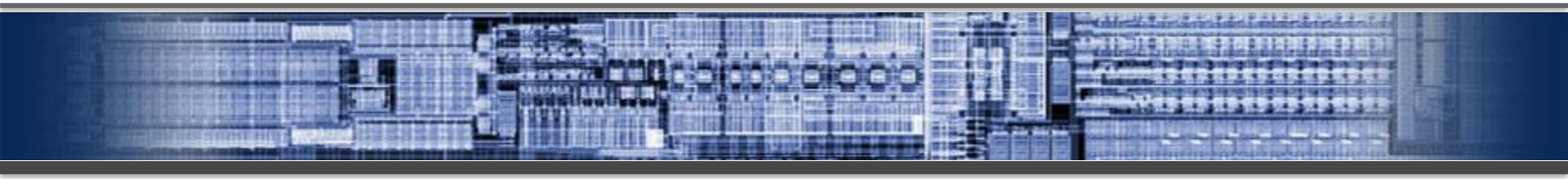
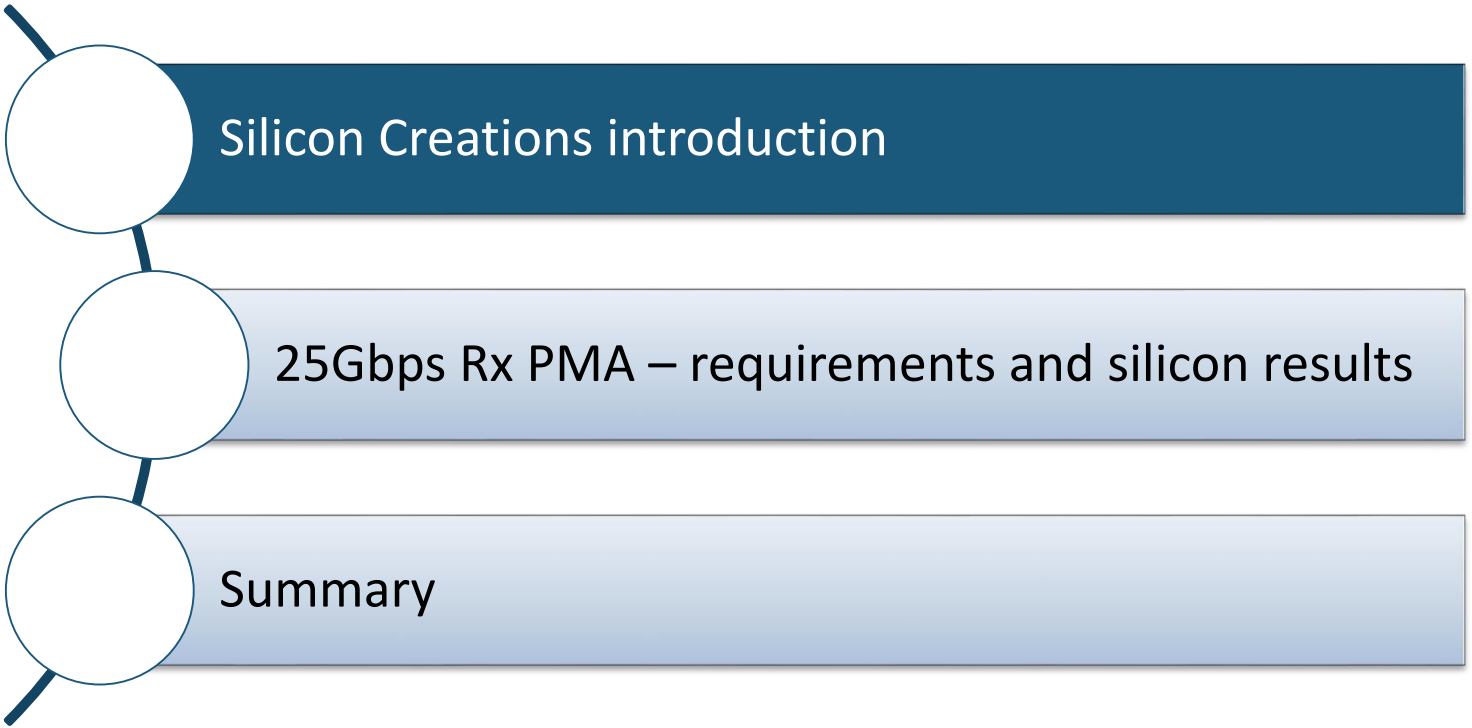


Comparing silicon to simulations for a 1.3pJ/bit 25Gbps SerDes Rx in TSMC 28HPC+

Andrew Cole, Blake Gray, Jeff Galloway at Silicon Creations

Outline


Silicon Creations introduction
25Gbps Rx PMA – requirements and silicon results
Summary

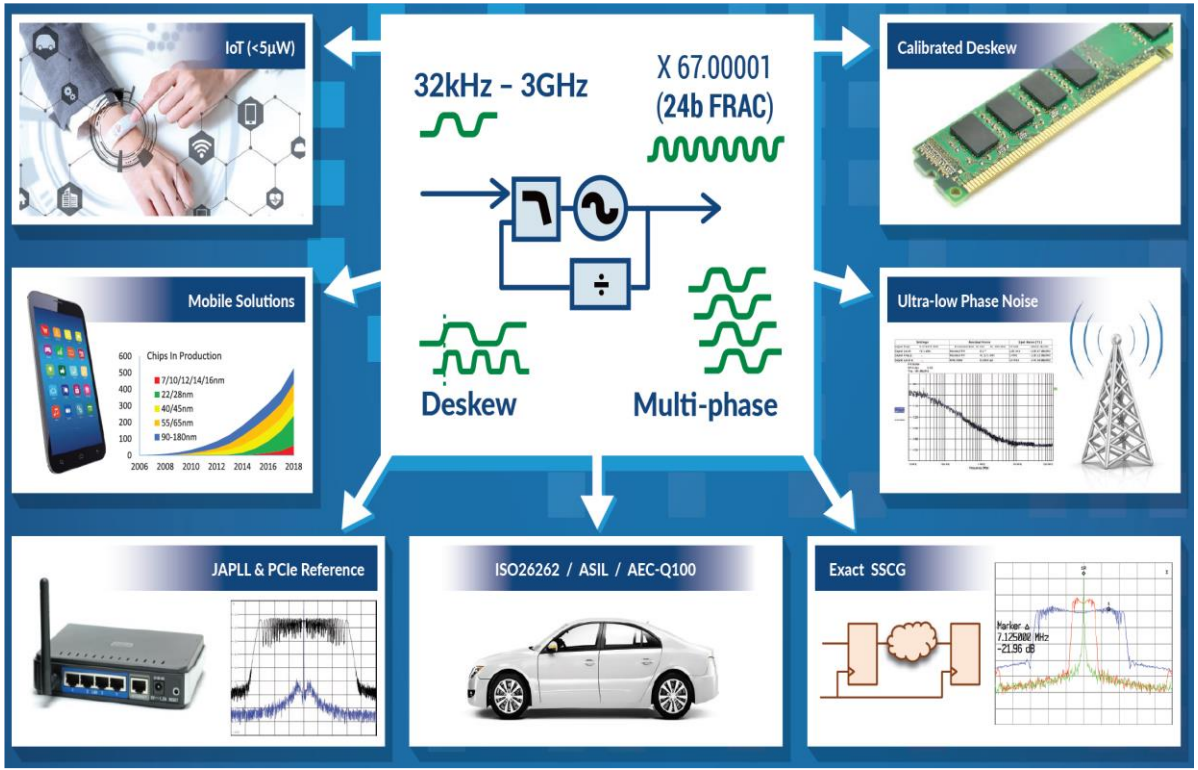
Silicon Creations Overview

- IP provider of PLLs, Oscillators and High-speed Interface
- Founded 2006 – self-funded, profitable and growing
- Design offices in Atlanta and Krakow, Poland
- High quality development, award winning support
- IP in mass production in TSMC from 7nm to 180nm, multiple 5nm PLLs delivered

PLLs from Silicon Creations

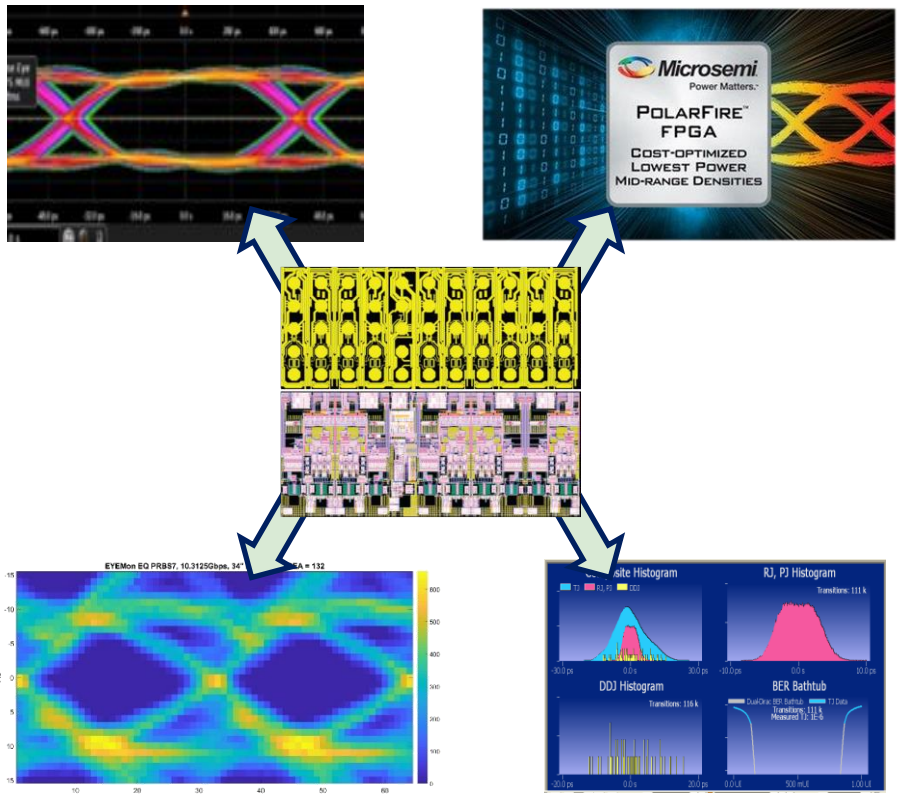
- Highest volume analog IPs – robust design and good QA are essential
  e.g. Fractional-N PLL:
  > 300 MP chips
  > 3M wafers
  … Many billions of these PLLs produced

- PLL products include general purpose, fractional, low jitter AFE, µW IoT, Automotive



SerDes from Silicon Creations

- Robust and proven from 28nm to 180nm and from <100Mbps to 25Gbps
- Multiprotocol (for FPGA) and targeted protocols
  - SGMII, XAUI, RapidIO, V-by-1 HS/US, CameraLink, FPDLink, JESD204, CPRI, PCIe1-4, 10G-KR, …
- Come to our booth to learn about our TSMC 12FFC/16FFC multiprotocol PMA

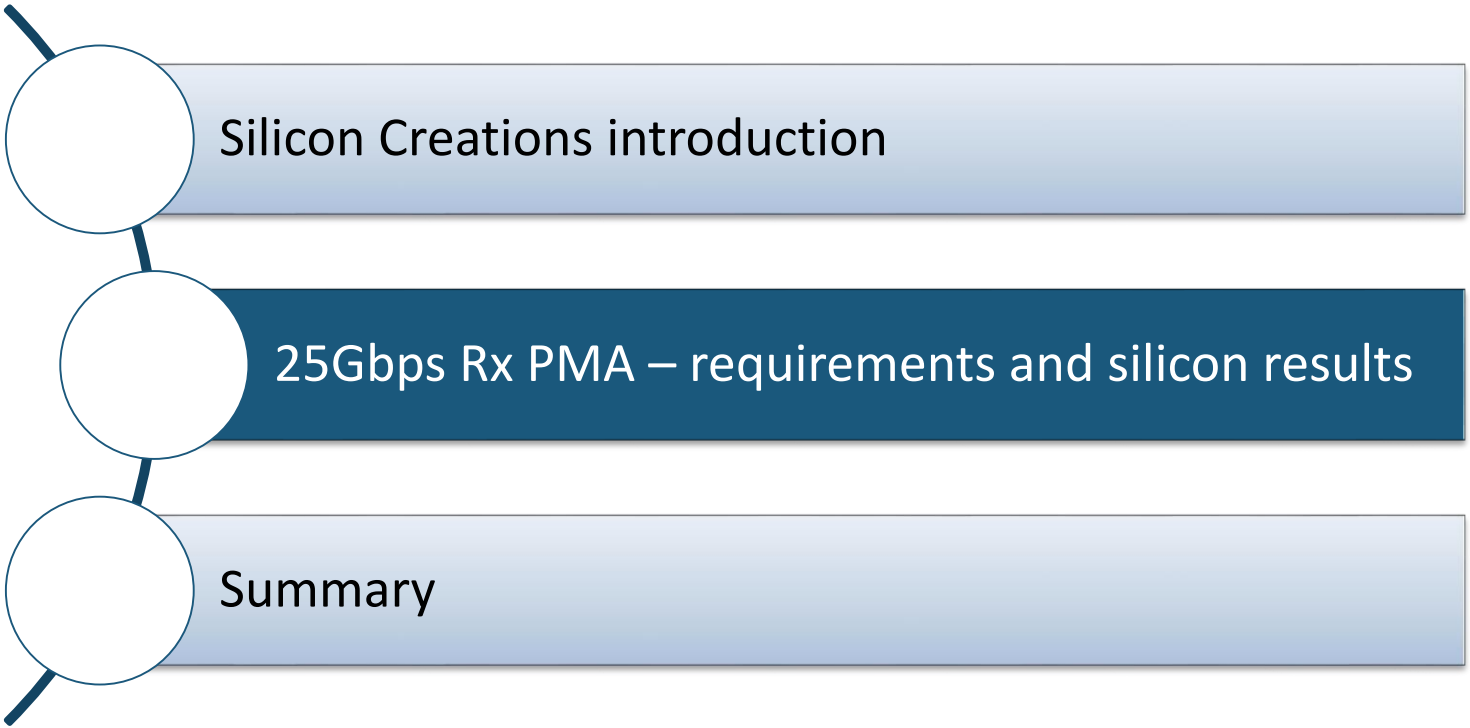


Awards for quality & support

TSMC

- 2018 & 2017: “Mixed-Signal IP Partner of the year”
- 2017: “Audience choice paper” – USA OIP
- 2014: “Best Emerging IP vendor”

Outline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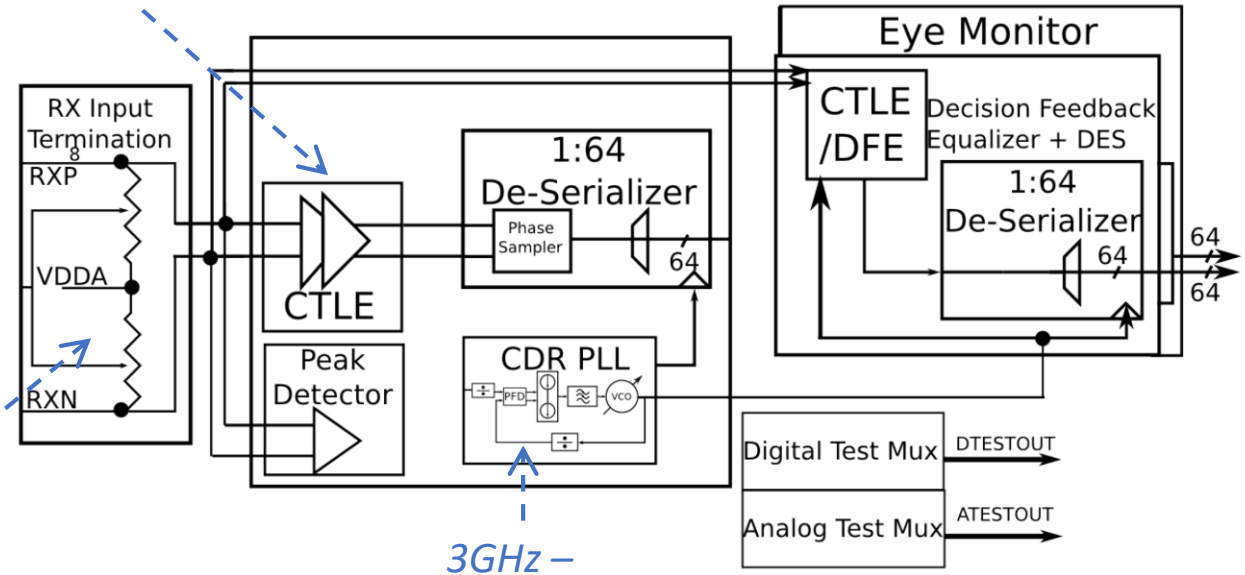
IP Requirements

- Customer chip needs to receive >5,000Gbps of data
- TSMC 28 HPC+ was determined by other circuits
- Chip will operate in limited temperature range, but has limited heat sinking
- Target power <2pJ/bit (mW/Gbps/lane) with >18dB (moderate loss) channel
- Following slides present our design and show how silicon is meeting the difficult power target

IP designed

Linear equalization

Long path: 5-tap DFE with 64-step Phase Interpolator and 32 step DC offset



Copy of DFE … sweep phase and compare data to DFE to measure eye

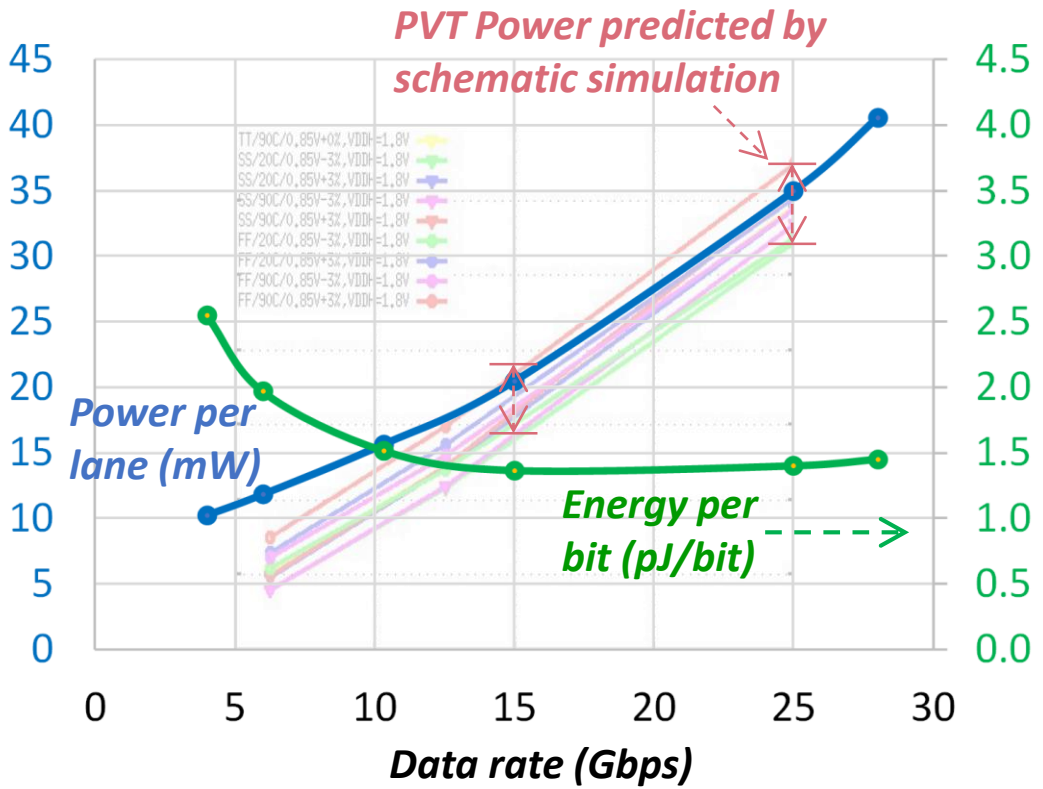
Termination with T-coil passive equalization

3GHz – 12.5GHz Ring PLL CDR

Turn off DFE and Eye for moderate loss (<18dB) channels

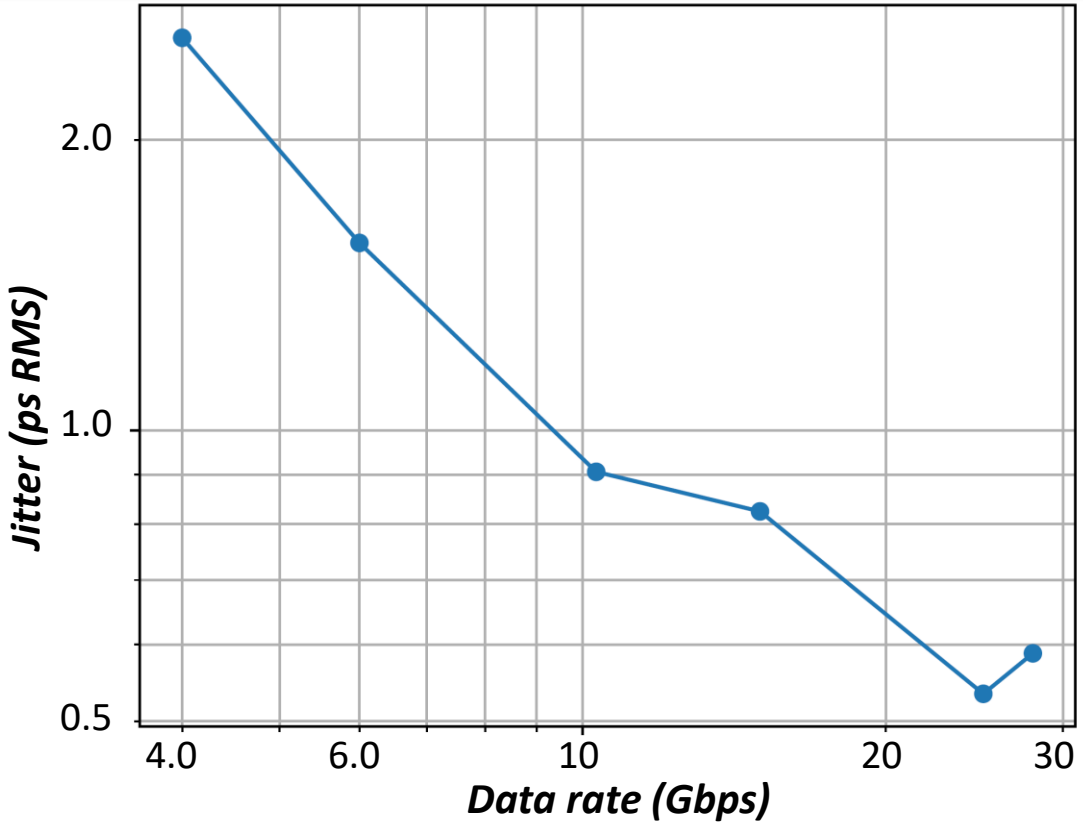
Power measurements

- Typical power measured with DFE off
- Simulations of extracted circuit predicted 1.3pJ/bit at 25Gbps (35mW/lane)
- Simulations and measurements with DFE on (supporting 25dB channel loss) show <2pJ/bit
- Silicon uses only 65% of 2pJ/bit design target for short channels
- Silicon works at 28Gbps over PVT



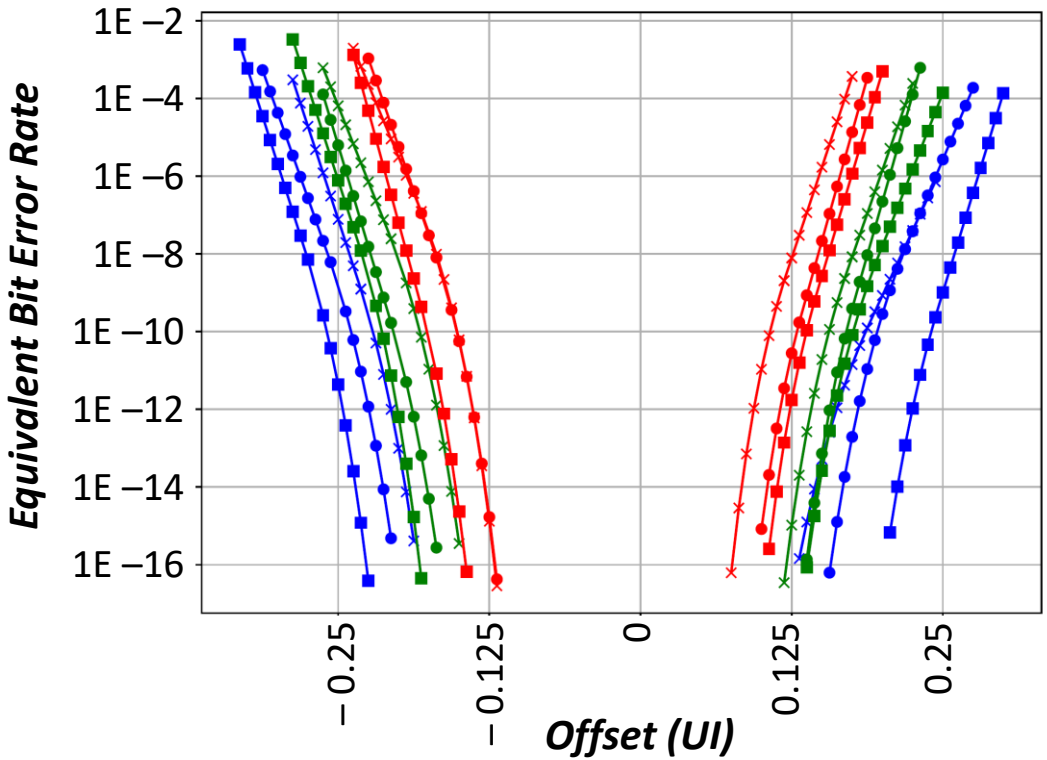
Jitter in recovered clock

- Ring PLL used for CDR balances power and performance
- Random jitter needs to be low enough for acceptable BER
- Results match expected jitter and are low enough for good BER over design range

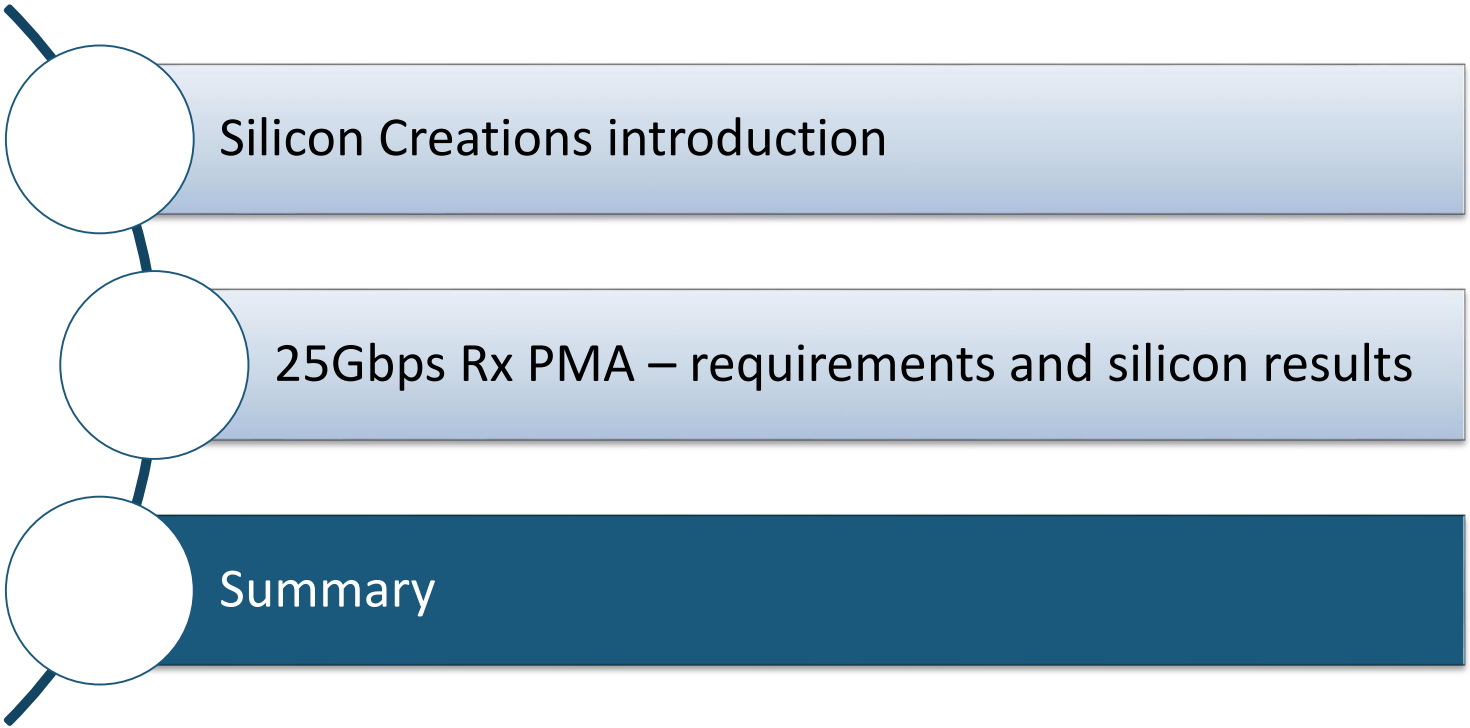


Bathtub at Slicer

- Eye monitor can be used to measure eye opening for large numbers of bits
- Measurements of eye opening with PRBS31 at 25Gbps after CTLE/DFE calibration with 16dB channel loss (20°C to 90°C)
- Results show expected closure with BER and plenty of margin over design range



Outline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Summary

- Silicon Creations has been providing reliable, high performance clocking and SerDes solutions since 2006
- Our IP is in very high volume production from 7nm, and already delivered to customers in TSMC 5nm FinFET
- Our versatile ring PLL has excellent PPA, and this has enabled us to build a 25Gbps SerDes receiver in TSMC 28 HPC+
- This receiver beats our lead customer's aggressive power target and operational range with acceptable margin