Increasing Analog Complexity is a Reality for Next Generation Chips

Randy Caplan
CEO and Co-founder
Silicon Creations

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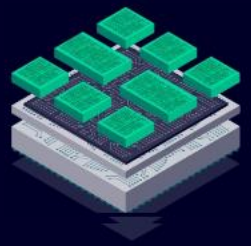
Latest Technology Trends That Are Influencing Next-Generation Semiconductor Chips

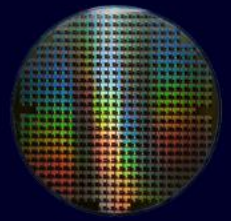
Die Evolution



ICs Growing in Die Size, Complexity

- Larger SoC / ICs, chiplets
- 3D-IC designs high-bandwidth memory

Process Technology Evolution



Silicon Manufacturing Technology Advancing

- New transistor types (FinFET, GAA)
- Device physics complexity increasing

Expanding IC Applications

AI / ML

Communications

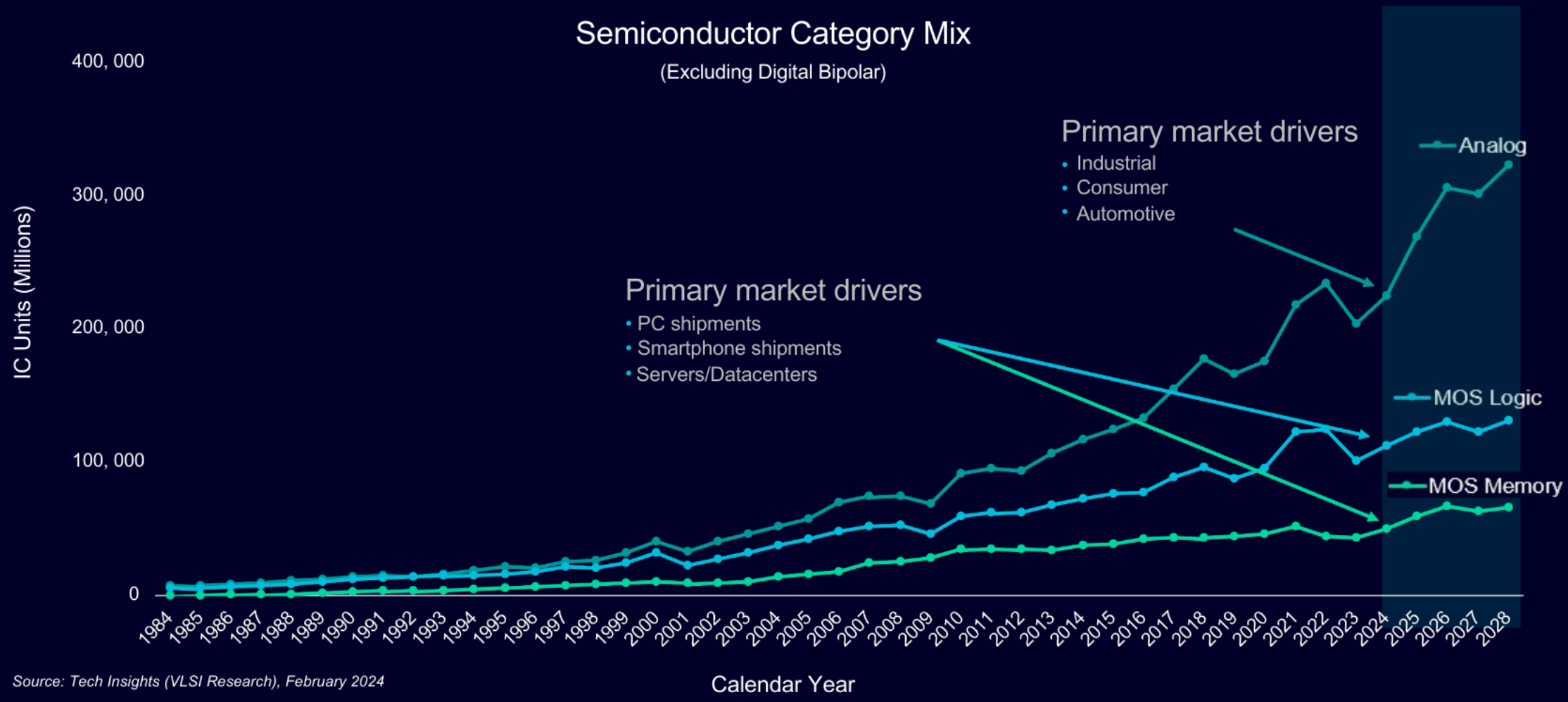
Server, HPC, Cloud

Healthcare

Internet of Things

Automotive

IC Unit Shipments Are Starting to Accelerate Across Major IC Markets: History and Forecast of Analog, Logic, and Memory Units



Source: Tech Insights (VLSI Research), February 2024

Die Evolution:
Monolithic to Multi-die

Chiplet A

Multiple Specialized PLLs

Clock Distribution

DDR Controller

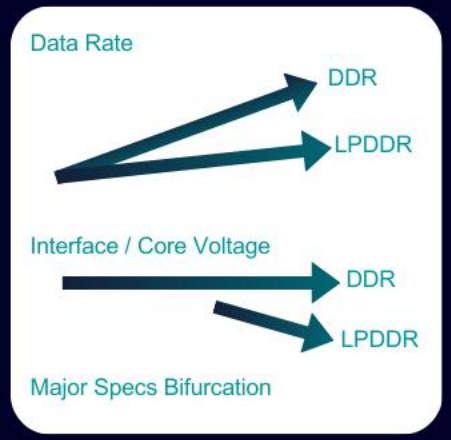
Chiplet B

RF DAC/ADCs

NRZ / PAM4 C2C Interface

Memory Chips

UCIE D2D Interfaces



Heterogenous Technology Chips

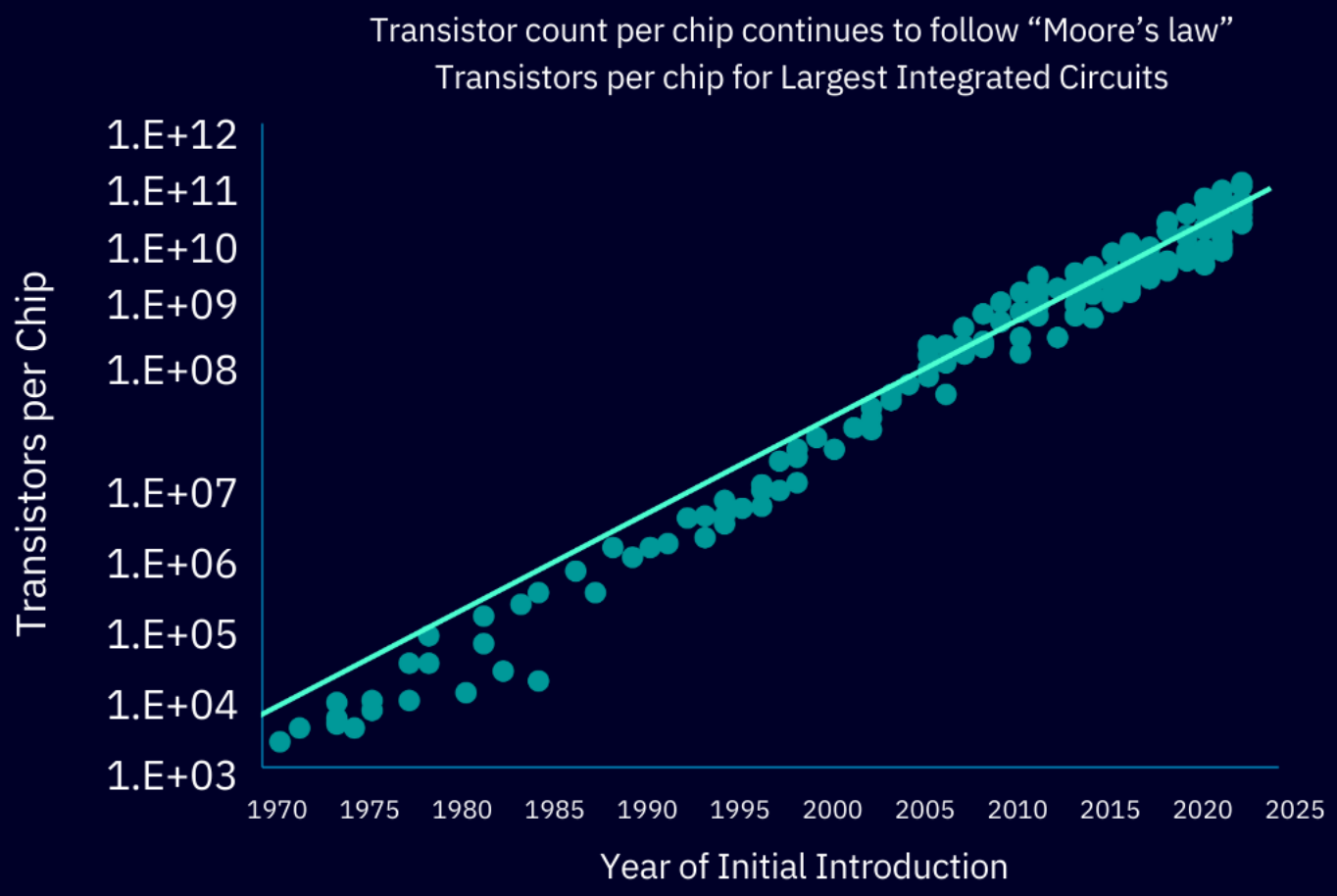
3D / 2.5D Advanced Packaging

Supplementary I/O Dies

UCIe
Universal Chiplet
Interconnect Express

IC Complexity is increasing with advanced analog and digital architectures
Die and package architectures are evolving fast to enable low latency and high data throughput

Process Tech Innovations Continues for Power, Performance, and Area Benefits



Foundries Continue to Innovate

tsmc SAMSUNG

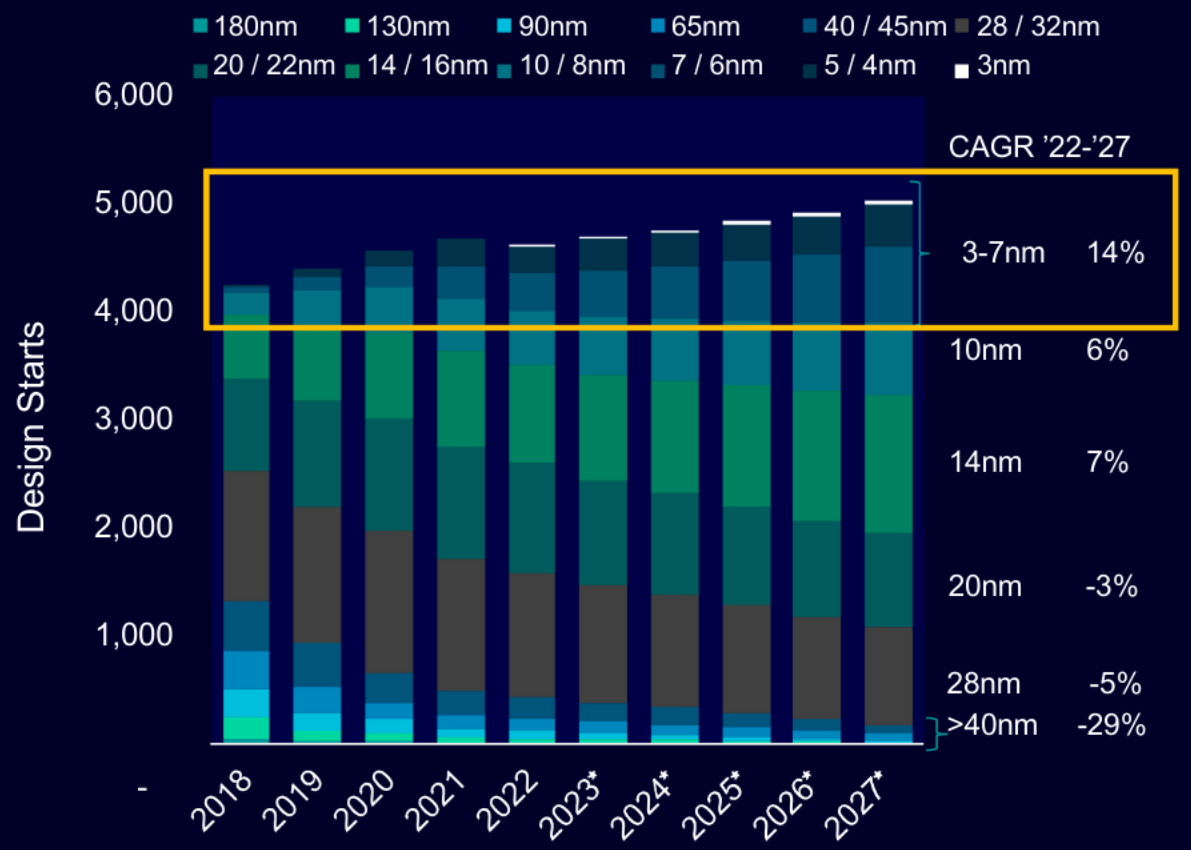
intel foundry Rapidus

Gate-All-Around (GAA)
The Next Evolution from FinFETs

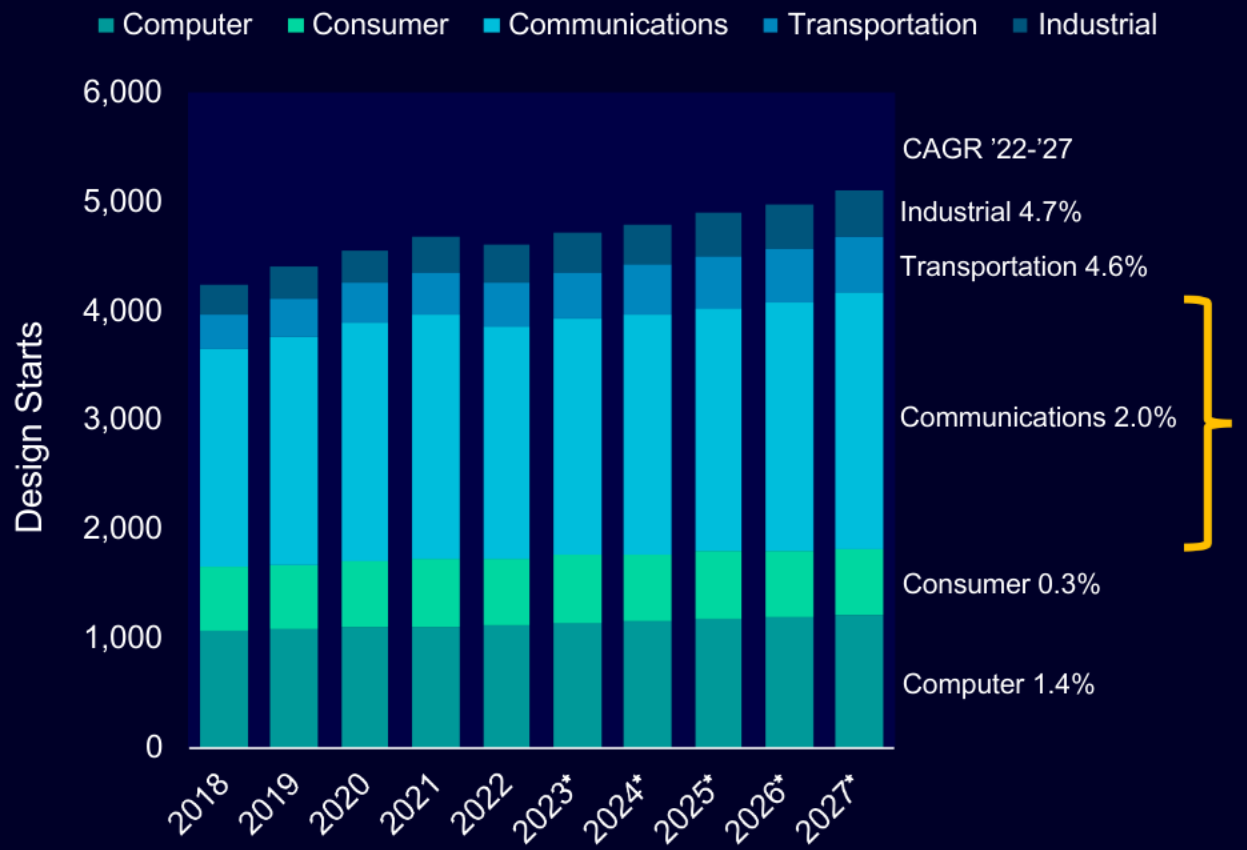
Source: Data source: Wikipedia (Wikipedia.org/wiki/Transistor_count) and OurWorldin Data.org (November 2023)

Advanced Performance Multi-Core SoC Design Starts
New Node Starts Are Rising, Communications Design Starts Dominate

Design Starts Across Process Tech Nodes



Design Starts by Industry



Source: Semico Research, March 2023

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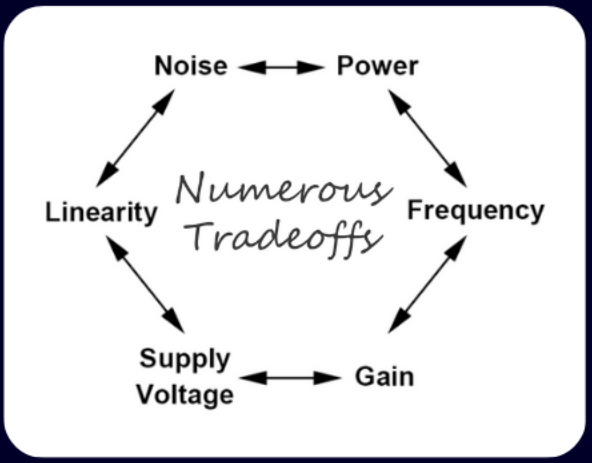
Analog Designs Are Widespread with Wide Variety of Circuit Types
Each Technology Shift Typically Requires Customization with Lowering Voltages

CML receiver	VREG	IREF	ADC	ESD
Loop Filter	Freq divider	DAC	Thermal Sense	CML Driver
Power Amp	Charge pump	Delay Line	Volt translator	Rectifier
Mixer	Phase-Freq det	LNA	Transmitter	Crystal Osc
RF Switch	LC VCO	CTLE	Bandgap	DFE
Ring VCO	Phase rotator	FFE	Lock detect	Signal Decap

Analog Circuit Architectures Continue to Evolve

Meet stringent functionality requirements
Be robust with circuit congestion and noise



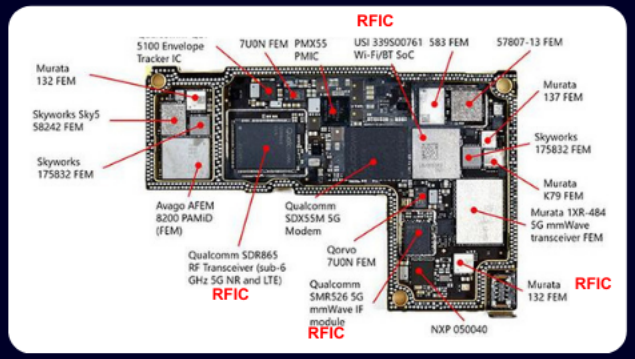
Analog Systems

- Wireless Transceivers
- Wired Transceivers
- Phase locked loop
- Delay locked loop
- Multi-protocol IOs
- Data Converters
- Image sensors

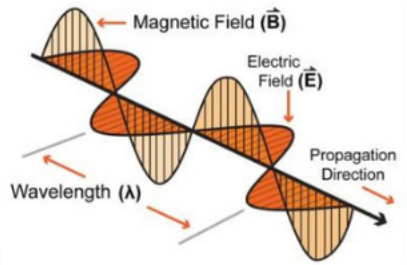
Moore's Law Keeps Delivering
Apple's Domain-Specific Processor Evolution

Year	2013	2015	2017	2019	2020	2022	2023
Phone	5s	6s	8 and X	11 & SE	12 Pro Max	14 Pro Max	15 Pro Max
Technology	28nm	14/16nm	10nm	7nm N7P	5nm N5P	4nm N4P	3nm N3B
Die Size	102mm^2	96mm2^	87.66mm^2	98.4 8nm^2	88mm^2	112.75mm^2	103.8mm^2
# of Transistors	>1 Billion	>2 Billion	4.3 Billion	8.5 Billion	11.8 Billion	16 Billion	19 Billion
CPU Performance Geekbench 1-Core	269	557	929	1331	1589	1879	2914
CPU Performance Geekbench Multicore	492 2 cores	1031 2 cores	2558 6 cores, + neural core	2558 6 cores, + neural core	4,250 6 cores, + 16 neural cores	5,455 2 HP CPUs 4 HE CPUs 5 GPUs 16 NPUs	7,199 2 HP CPUs 4 HE CPUs 6 GPU cores 16 NPUs

Sources: Teardown.com, Apple, Chipworks, ArsTechnica, Anandtech, Ifixit.com, wccftech.com – Tech Insights last updated 11/30/2023



Radio Frequency (3k Hz to 300 GHz) requires careful design handling



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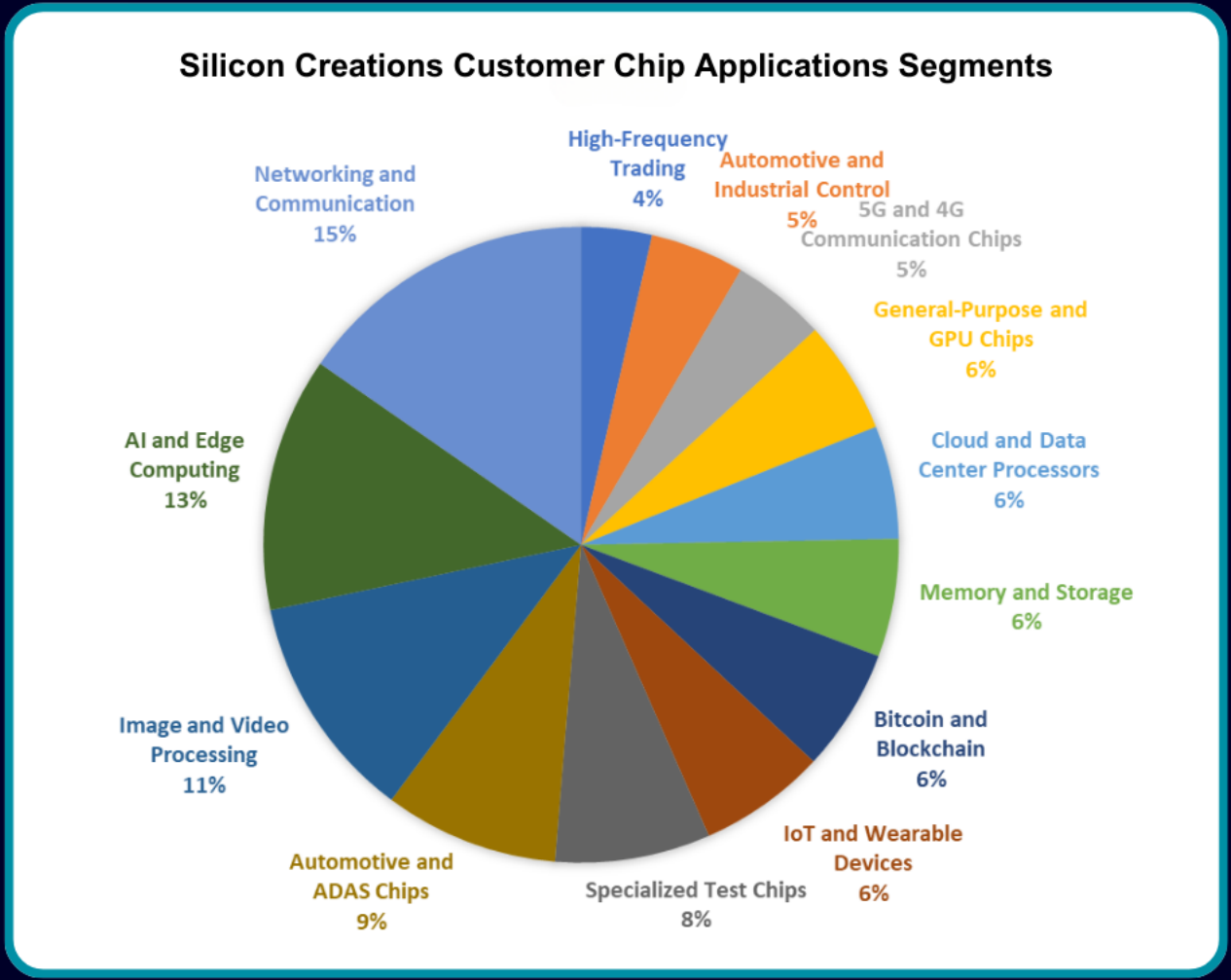
Silicon Creations Customer Chip Applications



Chip Applications	Count
High-Frequency Trading	15
Automotive and Industrial Control	20
5G and 4G Communication Chips	20
General-Purpose and GPU Chips	24
Cloud and Data Center Processors	24
Memory and Storage	25
Bitcoin and Blockchain	26
IoT and Wearable Devices	27
Specialized Test Chips	33
Automotive and ADAS Chips	37
Image and Video Processing	48
AI and Edge Computing	54
Networking and Communication	64
Total Number of Design Starts	**417**

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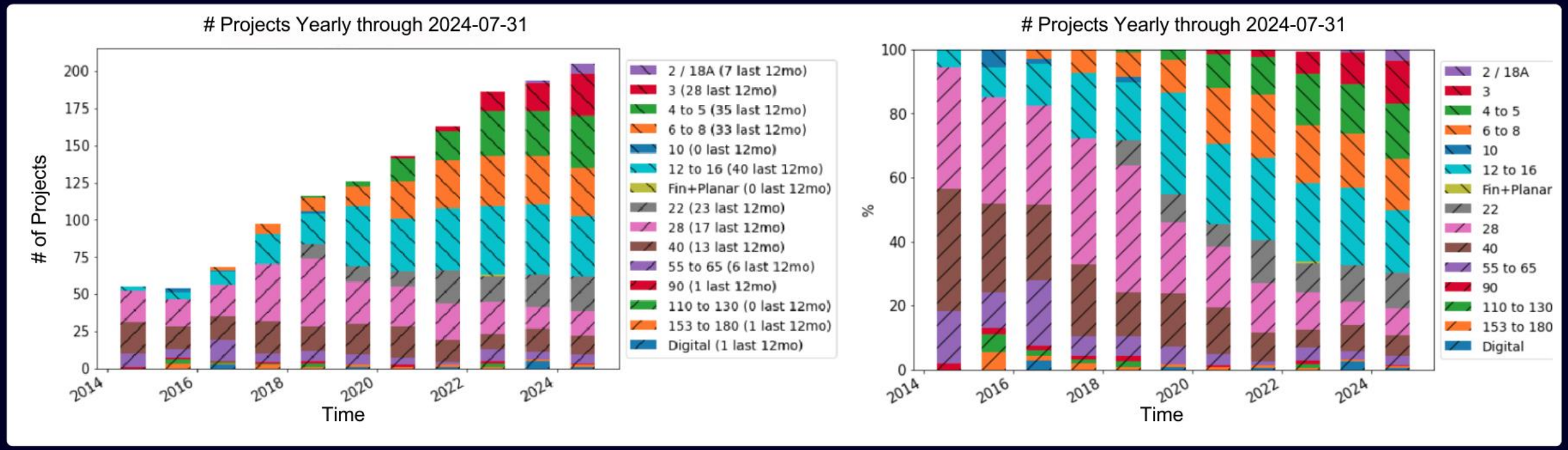
Silicon Creations' Customer Projects Track Industry Trends

- In 2020, half of all customer design starts (SoCs) were in planar
- Today roughly 2/3 of customer projects are being developed in FinFET
- Early adopters of most advanced nodes are less than few % in the first year of process availability



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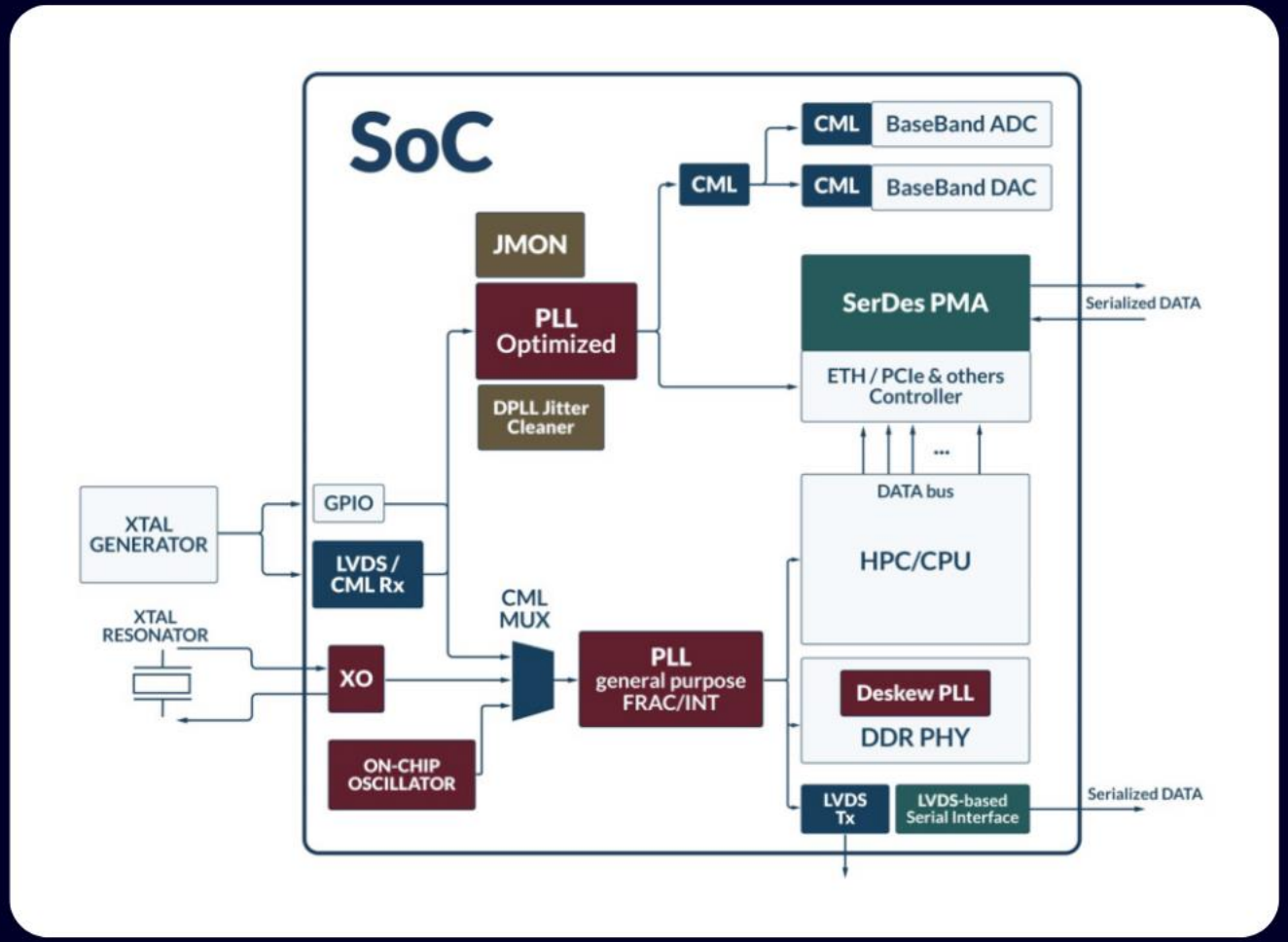
Silicon Creations
IP in today's SoC



General-Purpose &
Specialized **PLLs + RTL**
upgrades

High-Performance
LVDS I/O

Multiprotocol
SerDes PMA

Oscillators & XO

CML cells
for On-Chip Signaling

Temperature Sensors

Silicon Creations in Numbers

1500+
Chips using our IP

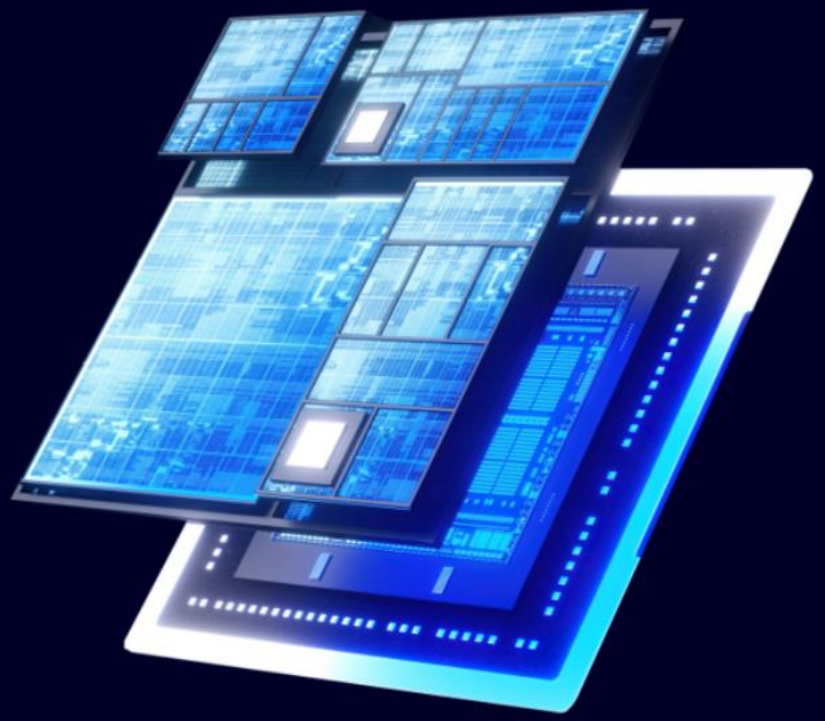
10M+
12" wafers shipped using our IP

700+
Unique IP Products

450+
Customers

150+
Production tape-outs annually

2nm
Under Development



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Foundry Collaboration

Collaboration with market-leading foundries is essential

Early stage PDK Access of leading-edge process nodes allows for silicon-proven IP ready for customers' first tape-out

tsmc GlobalFoundries intel foundry SAMSUNG UMC Rapidus

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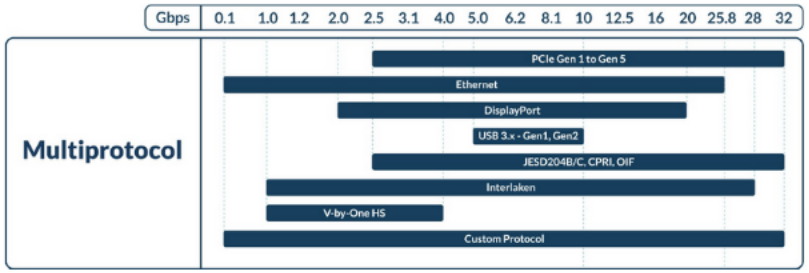
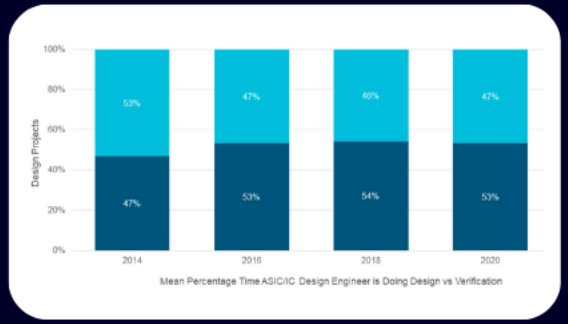
Challenges in Analog IP Design Today

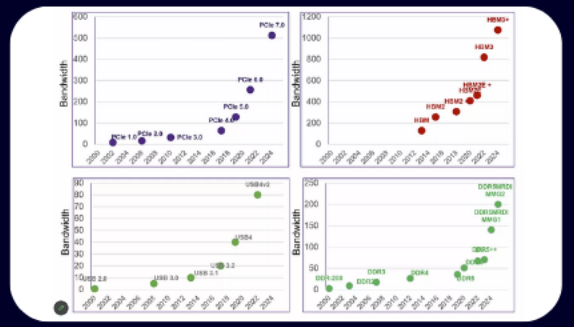
Need for more **specialized (modular, often digitally-assisted**, analog IP



Multiprotocol PMA support for higher data rates
-Transistor count of complex analog blocks exploding
-Advanced nodes require resource-hungry RC extraction

Growing device count and speed **challenge existing verification methods** and their runtime





IP Reliability in **advanced nodes** is more simulation intensive

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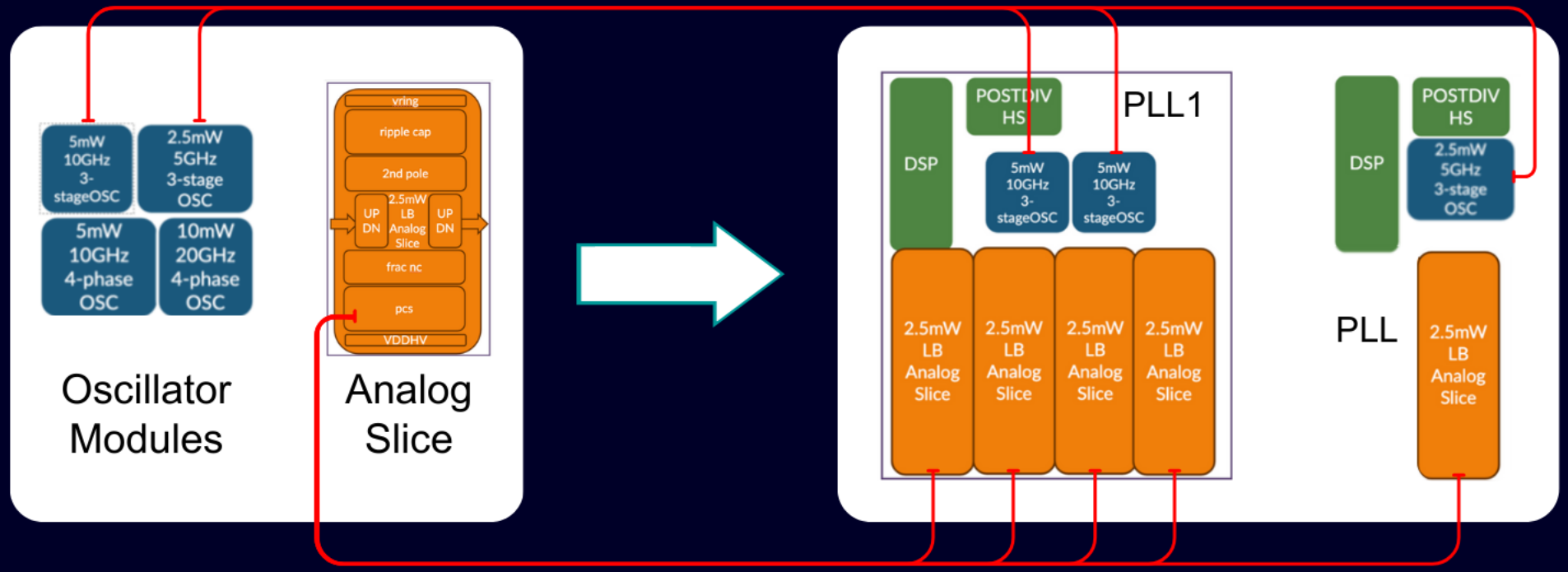
Modular Design Required to Keep Up with Complex SoCs

Challenges:
- DDR & D2D PHYs require specialized PLLs
- IP Portfolio has to grow -> modular design essential for design & long-term maintenance

Solution: Apply chiplet concept to IP….mix-n-match modules



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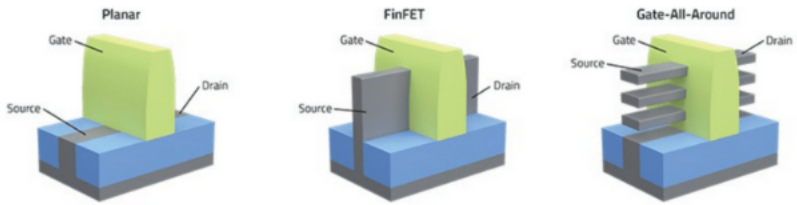
Advanced Node Challenges

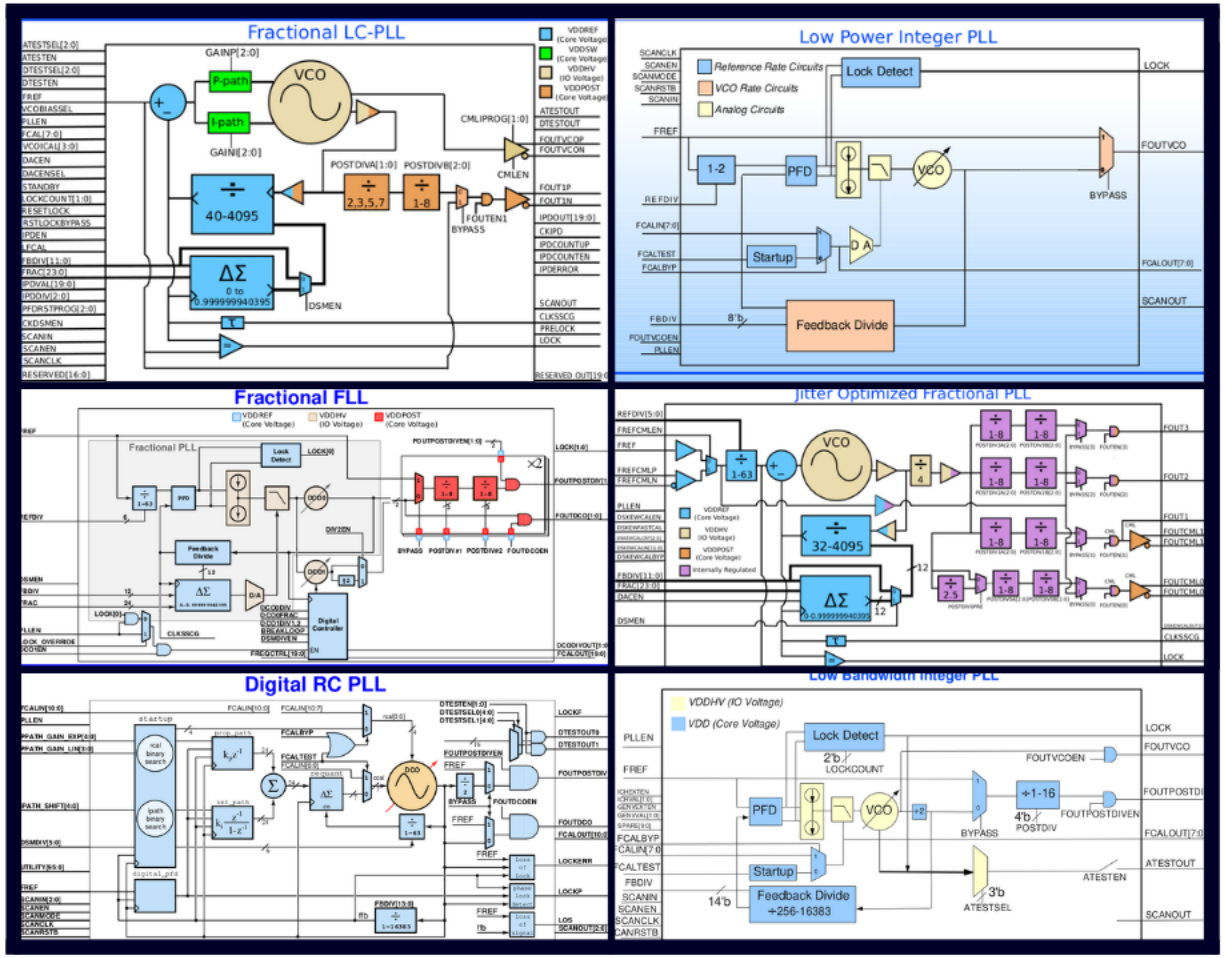
Technology challenges for analog design include:

- **Reduced or unavailable I/O voltage level**
  - Advanced cascoding to allow higher supply voltage
- **Growing Leakage & Noise (in particular 1/f)**
  - Hybrid MOS-R devices
- **Tighter design space to pass EMIR checks**
  - More budgeting for EMIR and performing analyses earlier
- **More complex DRC rules**
- PDK shifts for early adopters



- More Design & Analyses Overhead per IP product
- More **Computing Power**
- More **Advanced Software**
- Skilled **Engineers**

Clocking IP Features / Flavors - Increasing Complexity with Multiple Architectures



New Requirements

⬇

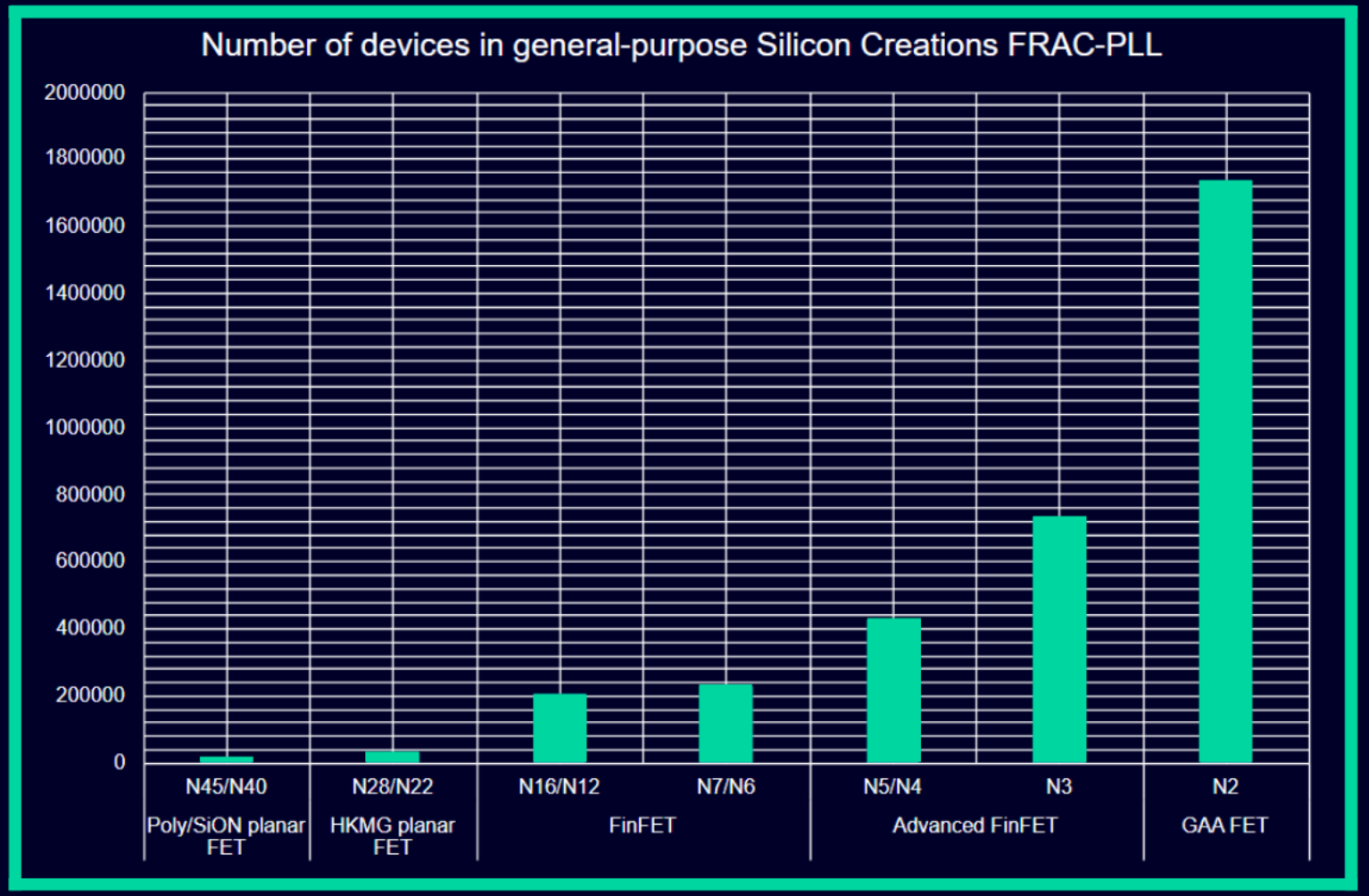
More specialized PLLs and clocking IPs

New and more "digital" options are being explored and many of them already been converted into mass production silicon.

Every generation comes with many flavors and that require **more and thorough SPICE simulations** to run.

SPICE simulation is a requirement, even for Digital PLLs.

PLL Design Challenges – Device Count



Number of devices required to create PLL is fast increasing due to fabrication constraints – in modern nodes there is only one minimum size transistor available

Good **analog circuit construction** requires **complex compound devices** to achieve target matching and noise performance

Those devices have **more and more complex models,** often with many effects not defined by BSIM models, hence requiring extra external modeling

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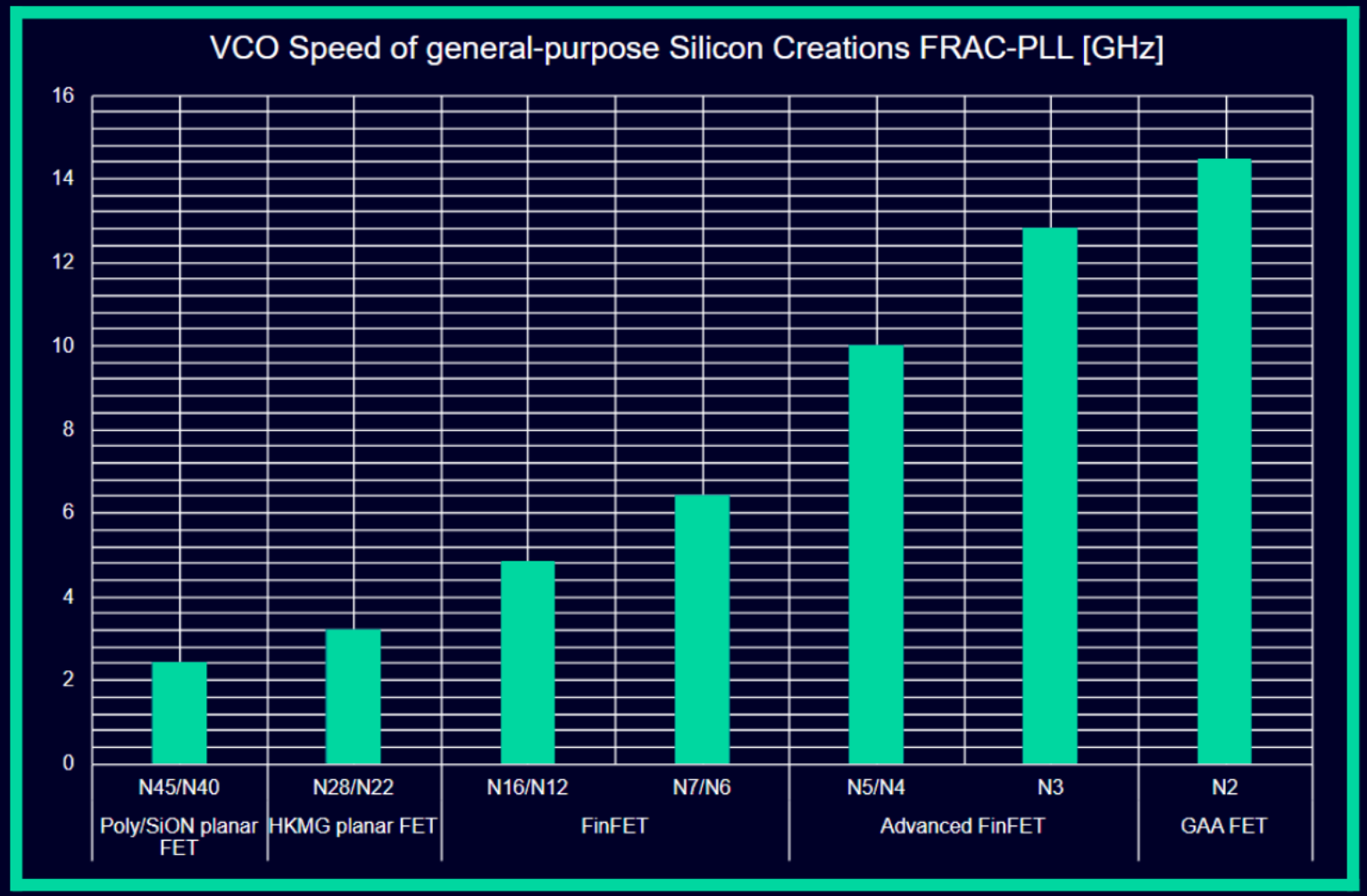
PLL Design Challenges
- Speed



Max VCO speed of most popular Silicon Creations FRAC-PLL variant in many nodes

Customers expect frequency increase in every generation so they can use single **'one-size-fits-all PLL'** in as many scenarios as possible

PLL speed defines how many simulation points are necessary

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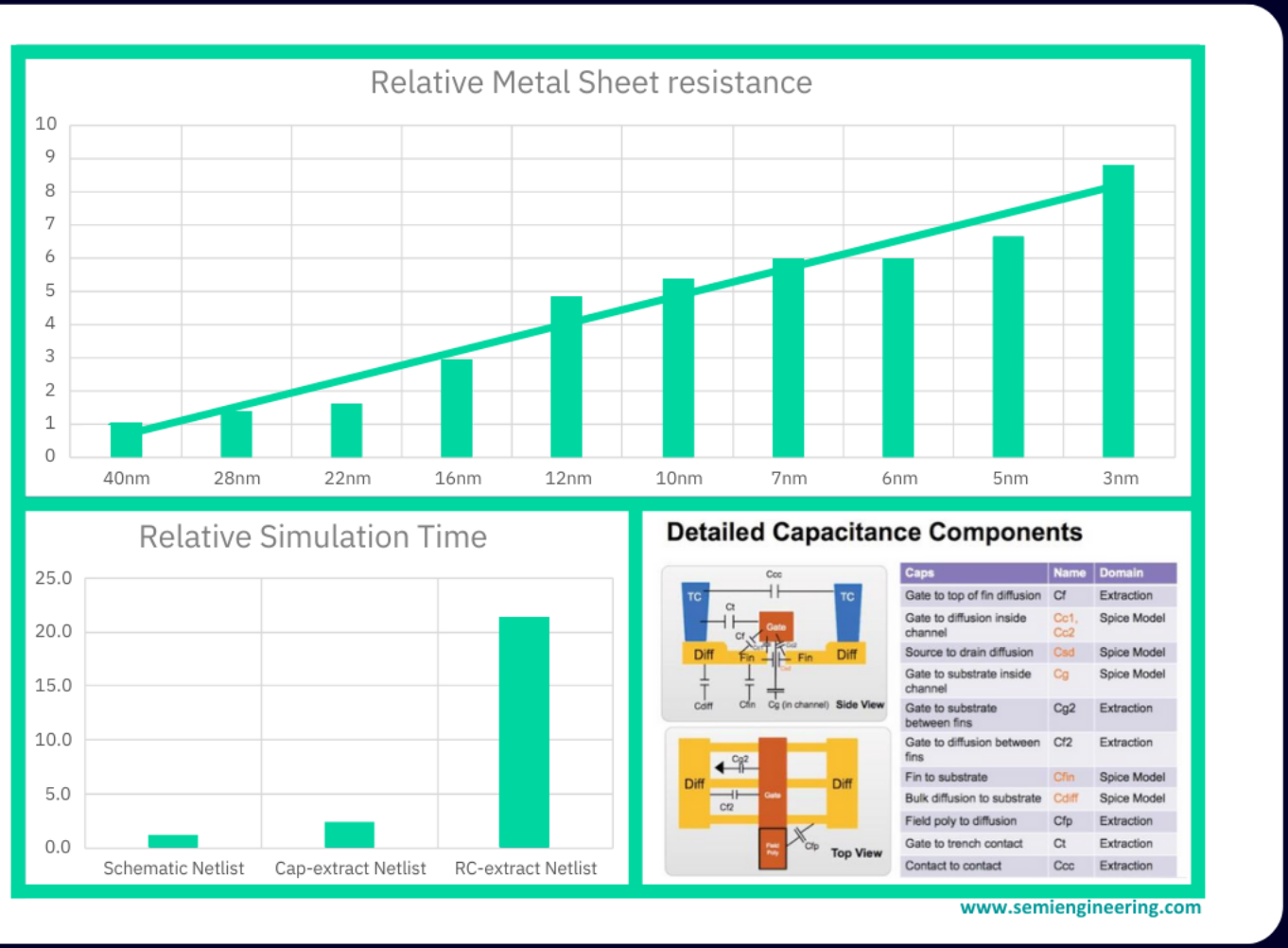
Constantly Growing Difficulties - RC Parasitics



Circuit Designers

Layout Engineers

Resistance kills performance even for DC circuits.

Further, simulating up to 8 RC extraction corners requires prep.

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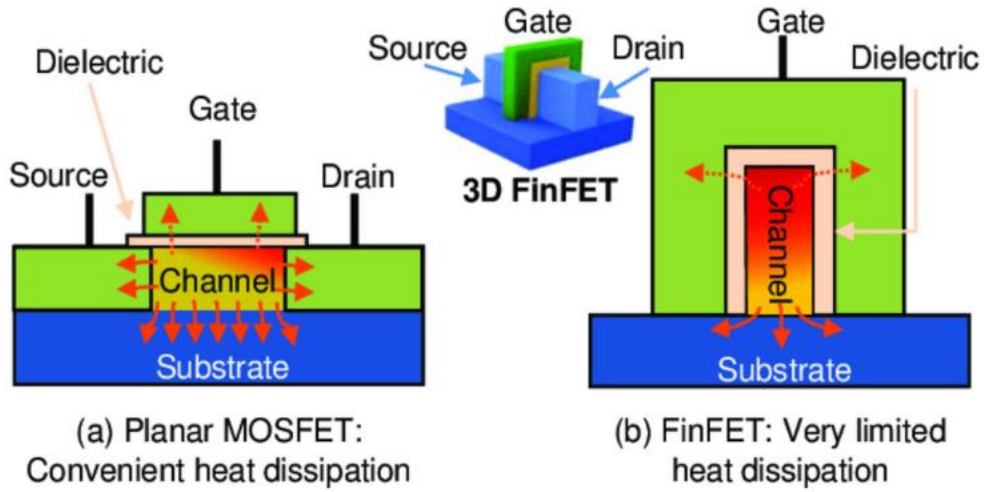
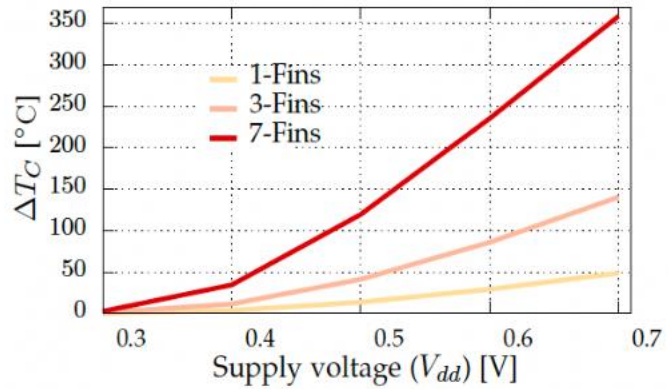
Constantly Growing Difficulties - Reliability



(a) Planar MOSFET: Convenient heat dissipation

(b) FinFET: Very limited heat dissipation

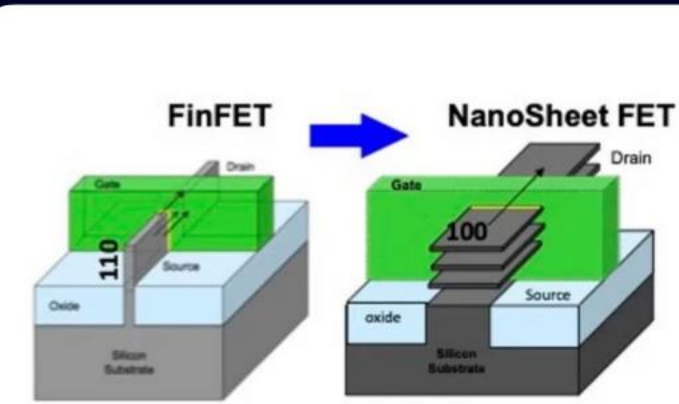


Aging Checks in SPICE Run at Every Block

- Self-heating (SHE)
- Real-time self-heating (RTSHE)

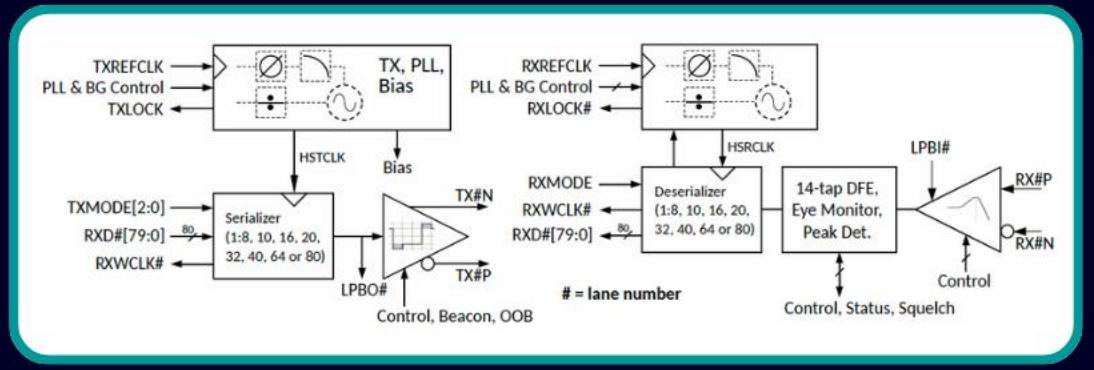
Electrical Overstress Assertions

- Short surges in small devices due to charge sharing and switching events
- Must be maintained within limits (SPICE)

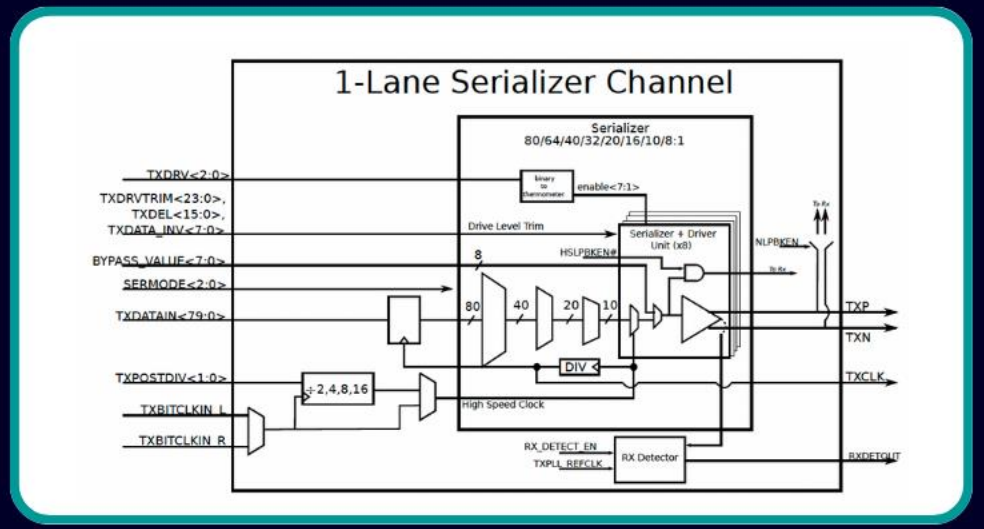


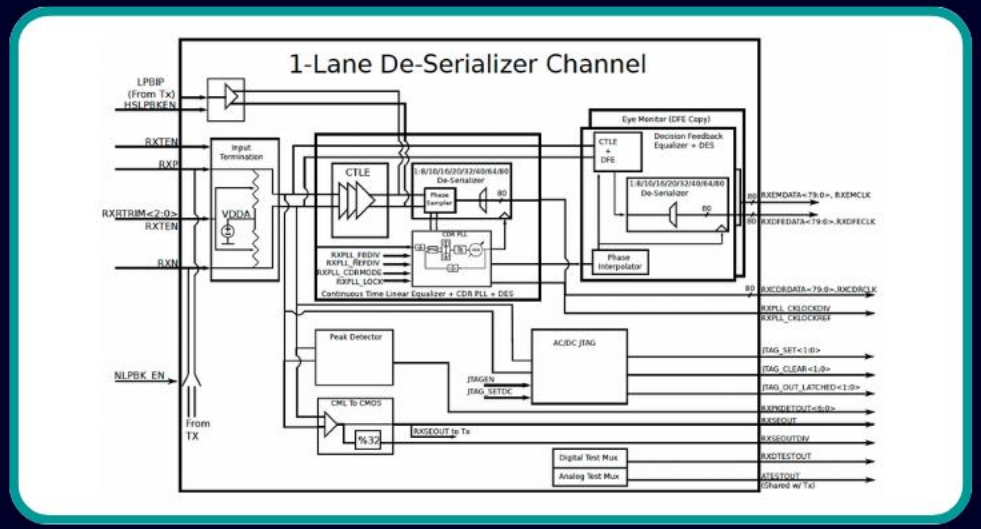
SerDes Design Challenges - Increasing Complexity with Multiple Architectures

Simple SerDes PMA Block Diagram…



…contrast with high analog complexity in Ser(Tx) & Des(Rx)





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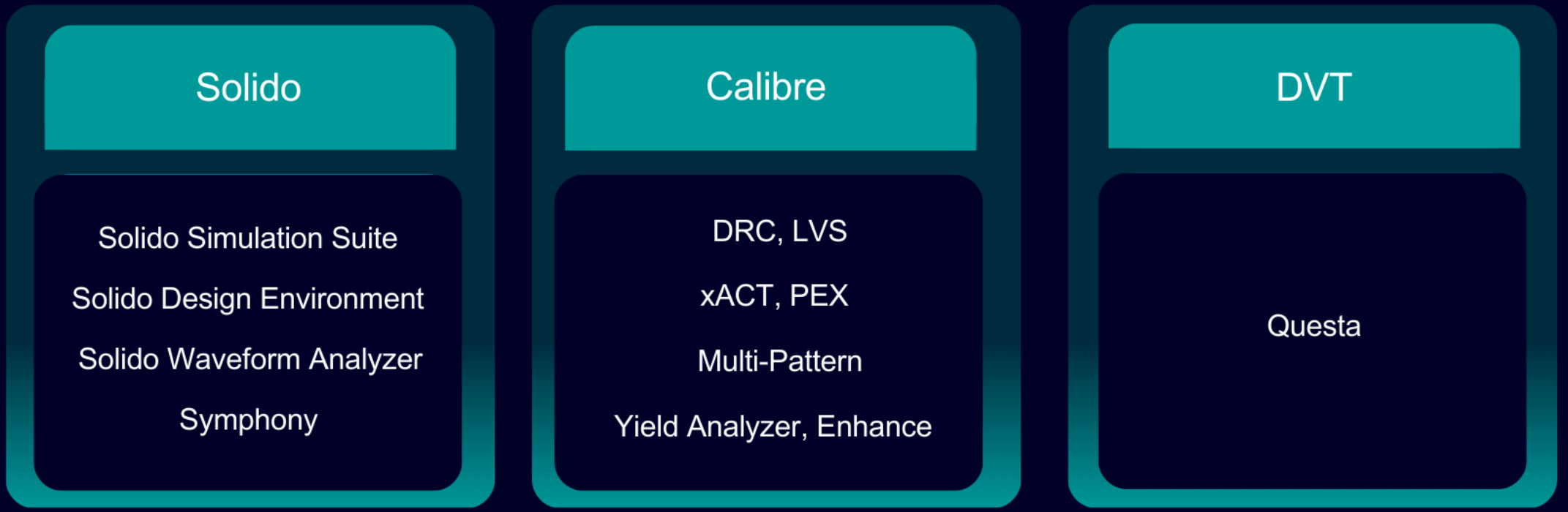
Silicon Creations and Siemens Partnership

Siemens EDA Technologies Utilized by Silicon Creations



Good collaboration in defining newer verification requirements for EDA development

Silicon Creations Endorsed Solido Simulation Suite Launch at DAC 2024

PRESS RELEASE

Siemens delivers AI- accelerated verification for analog, mixed-signal, RF, memory, library IP and 3D IC designs in Solido Simulation Suite

June 24, 2024
Plano. Texas. USA

"As a provider of top-tier silicon intellectual property for high-performance clocking and low-power/high-speed data interfaces, our products play a crucial role in modern SoCs," emphasized **Randy Caplan, CEO and Co-Founder of Silicon Creations**. "The complexity of designing at 5nm and below, coupled with slow post-layout simulations, due to very high device counts, poses major challenges. Fast and accurate simulation of GAA and FinFET process technology-based designs is imperative to meet our end-customers' demanding requirements and schedules. In our active participation in the early access program for Solido™ Simulation Suite, using various post-layout designs, we observed an impressive acceleration of up to 11X while preserving SPICE-level accuracy. We look forward to leveraging Solido Simulation Suite to validate our most complex designs, ensuring first silicon success and meeting our high-yield targets."

Siemens EDA technologies allows Silicon Creations to continue its IP journey into the Ångström Era