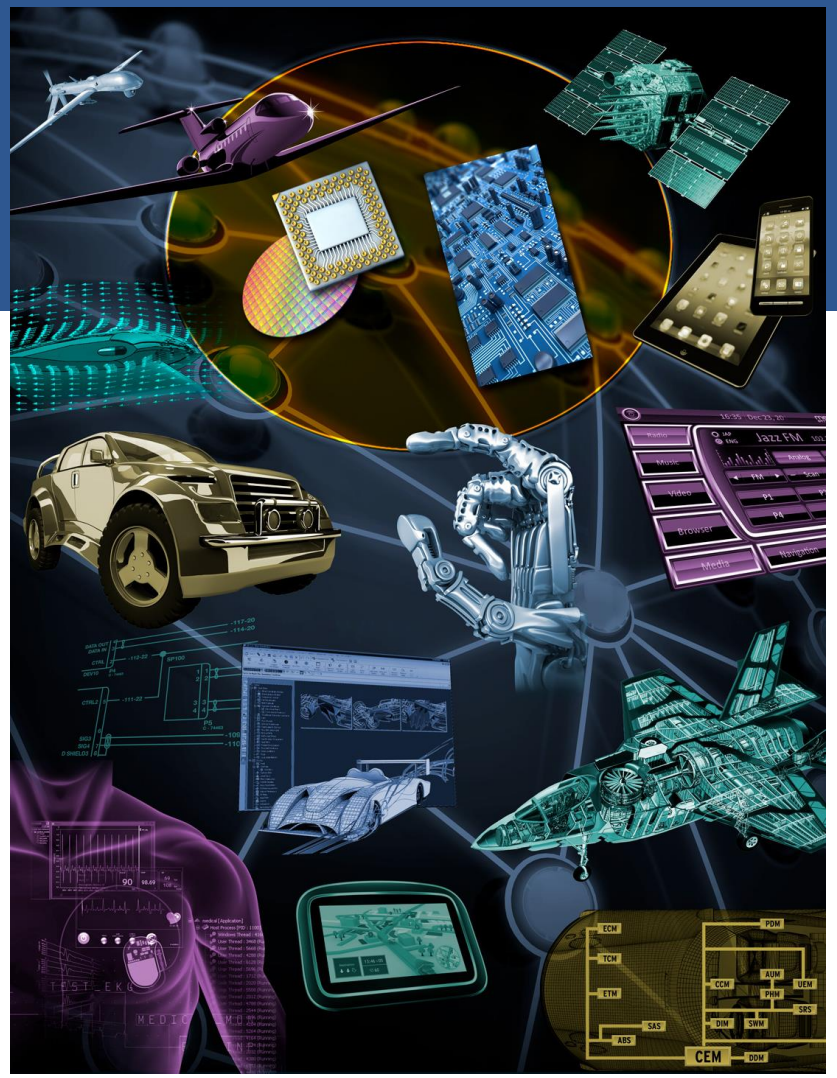

Silicon Creations and Calibre

Ensuring Silicon Results will Match Circuit Simulation

Andrew Cole

VP, Silicon Creations

Chris Clee

Product Marketing Manager, Calibre Parasitic Extraction Products

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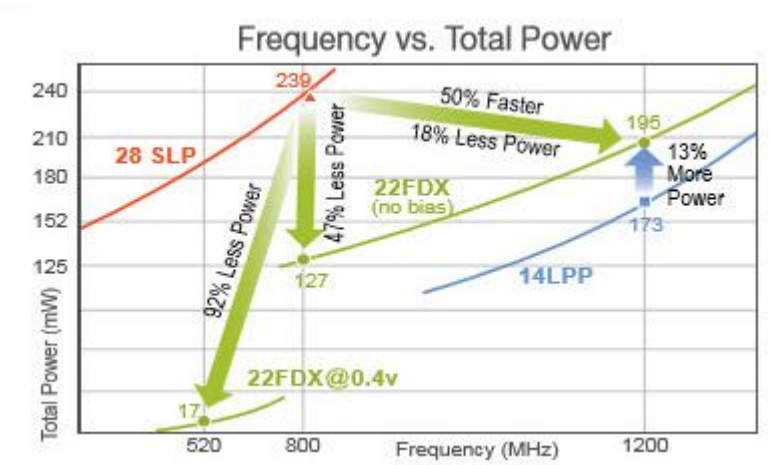
Agenda: Calibre xACT For Advanced Node Parasitic Extraction

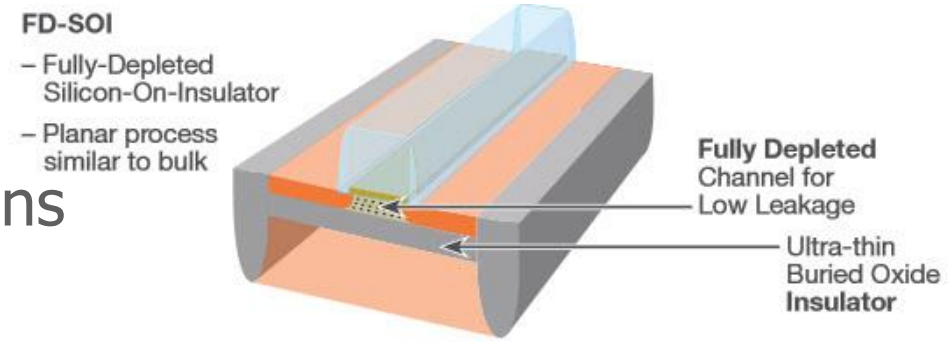
- Advanced node challenges
- Field solver vs. table-based approaches to extraction
- Impact of errors
- Calibre xACT hybrid approach to extraction
- Results: accuracy
- Product portfolio and flows

Problem Statement: Accurate Silicon Prediction
Efficient calculation and integration of circuit components

- New processes deliver power/performance/area benefit…
- …and require unprecedented modeling / simulation accuracy
  - Device characterization/parameter extraction
  - Interconnect modeling
  - Integration into design and simulation flows
  - Integrated solutions for RF design
- IP providers require early enablement
  - Develop on early versions of the PDK
  - IP needed early to drive customer applications
    - Mobile, high performance, automotive, etc.
  - Integration to enable best-in-class flows



Source: Globalfoundries



Source: Globalfoundries

Challenges Specific To 16nm And Below

Multi-patterning

- Misalignment between masks leads to unpredictability
- Impact on parasitics is layout-dependent
- Effectively adds corners to analysis
- Creeping up to the routing layers

FinFETs

- No "one size fits all" solution
- 3D effects contribute significantly to parasitics, disrupt profile

Local interconnect

- Enables greater density, smaller standard cells
- Necessitates 3D device models

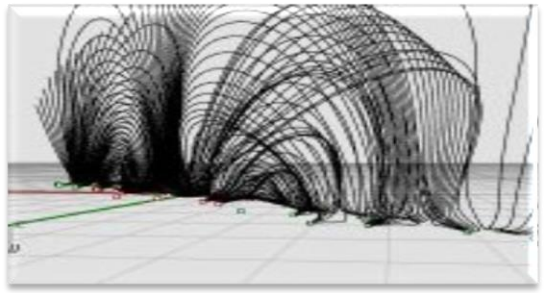
Rule-based Vs. Field Solver Approaches

Rule-Based / Table-based

- Measures distances between polygons, looks up values from pre-characterized tables
- Fast performance

$$C = \frac{\varepsilon A}{d}$$

Field Solver



- Solves Maxwell's equations
- Highest accuracy

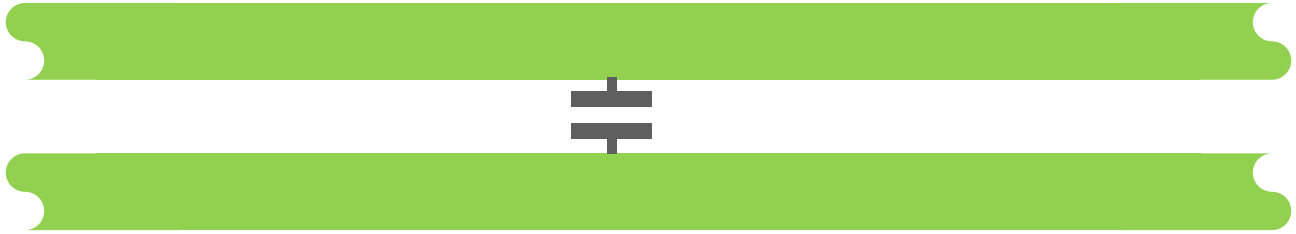
$$\vec{\nabla} \cdot \vec{E} = 0 \qquad \vec{\nabla} \times \vec{E} = -\frac{\partial \vec{B}}{\partial t}$$

$$\vec{\nabla} \cdot \vec{B} = 0 \qquad \vec{\nabla} \times \vec{B} = \mu\varepsilon \frac{\partial \vec{E}}{\partial t}$$

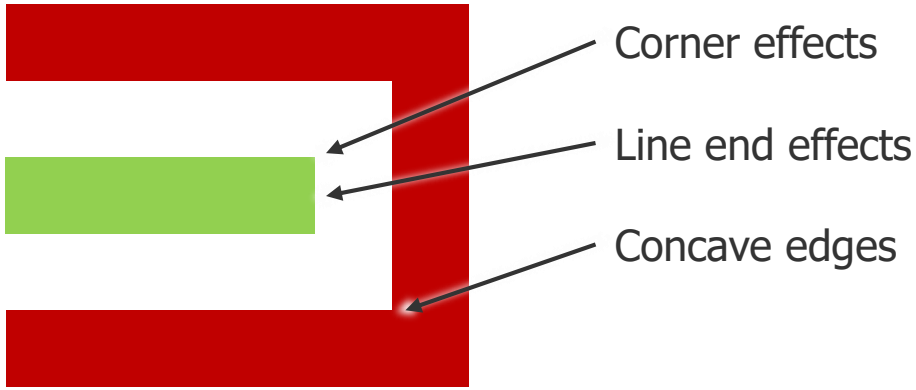
3D Line-End Effects

Long wires

$$C = \frac{\varepsilon A}{d}$$



Short wires



FinFET Challenges: Modeling MOL

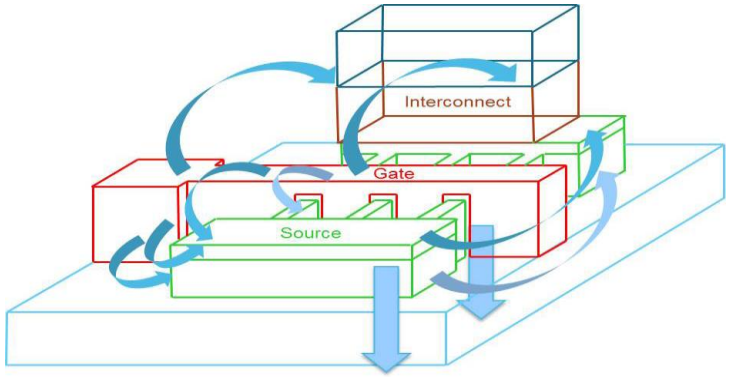
More Parasitic Effects

- Further refinement by foundries

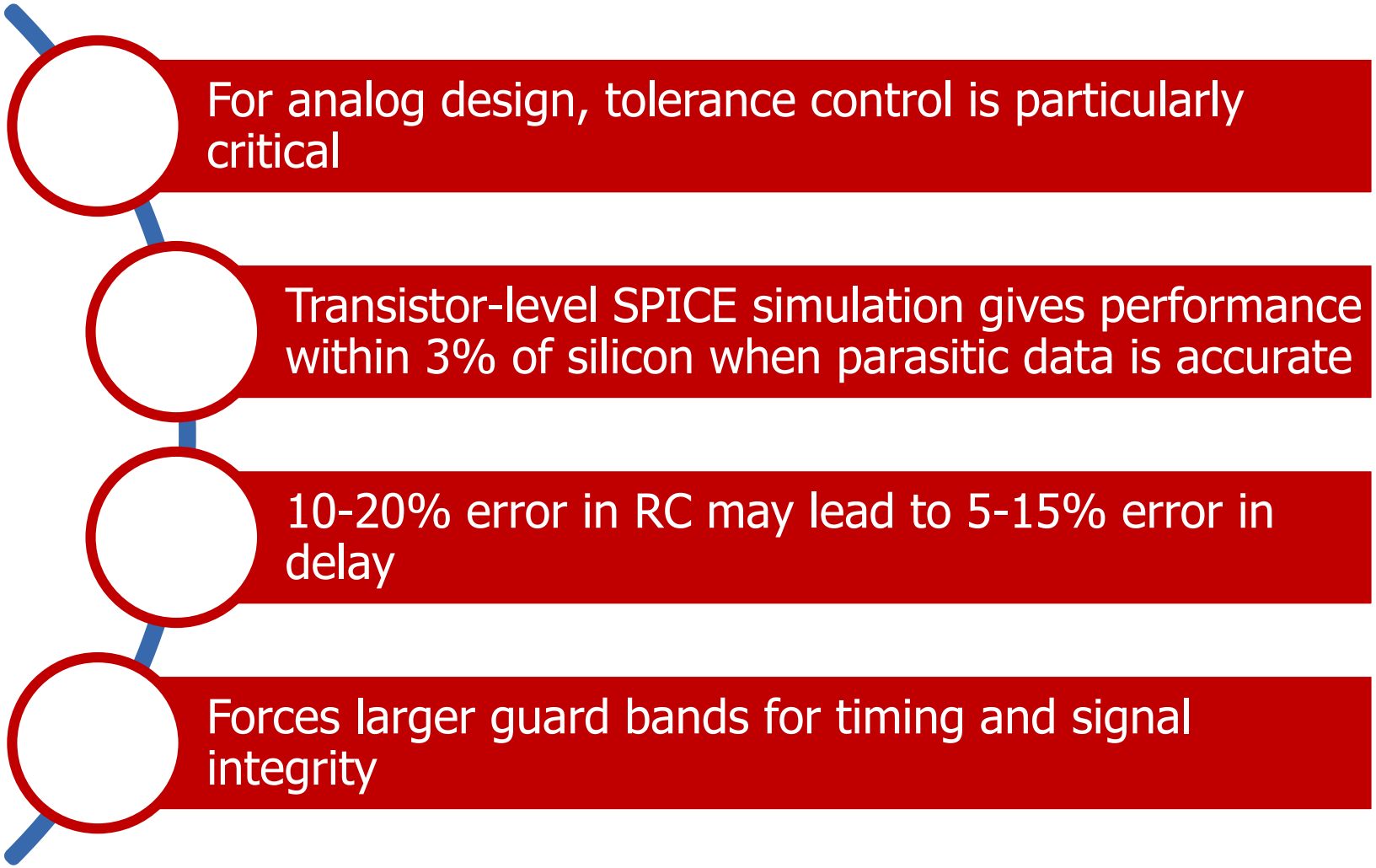
Complex Geometries

- Fin/poly/diffusion
- Local interconnect
- Contacts

Tighter Accuracy Requirements



Impact Of Extraction Errors



Calibre xACT For Full-Chip Design

A New Approach

Table-based

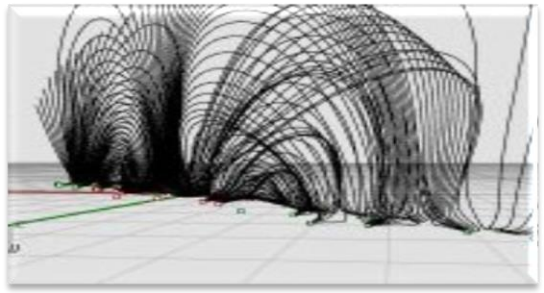
- Measures distances between polygons, looks up values from pre-characterized tables
- Fast performance

$$C = \frac{\varepsilon A}{d}$$

Hybrid Approach (Calibre xACT)

Best combination of performance and accuracy for advanced nanometer processes

Field Solver

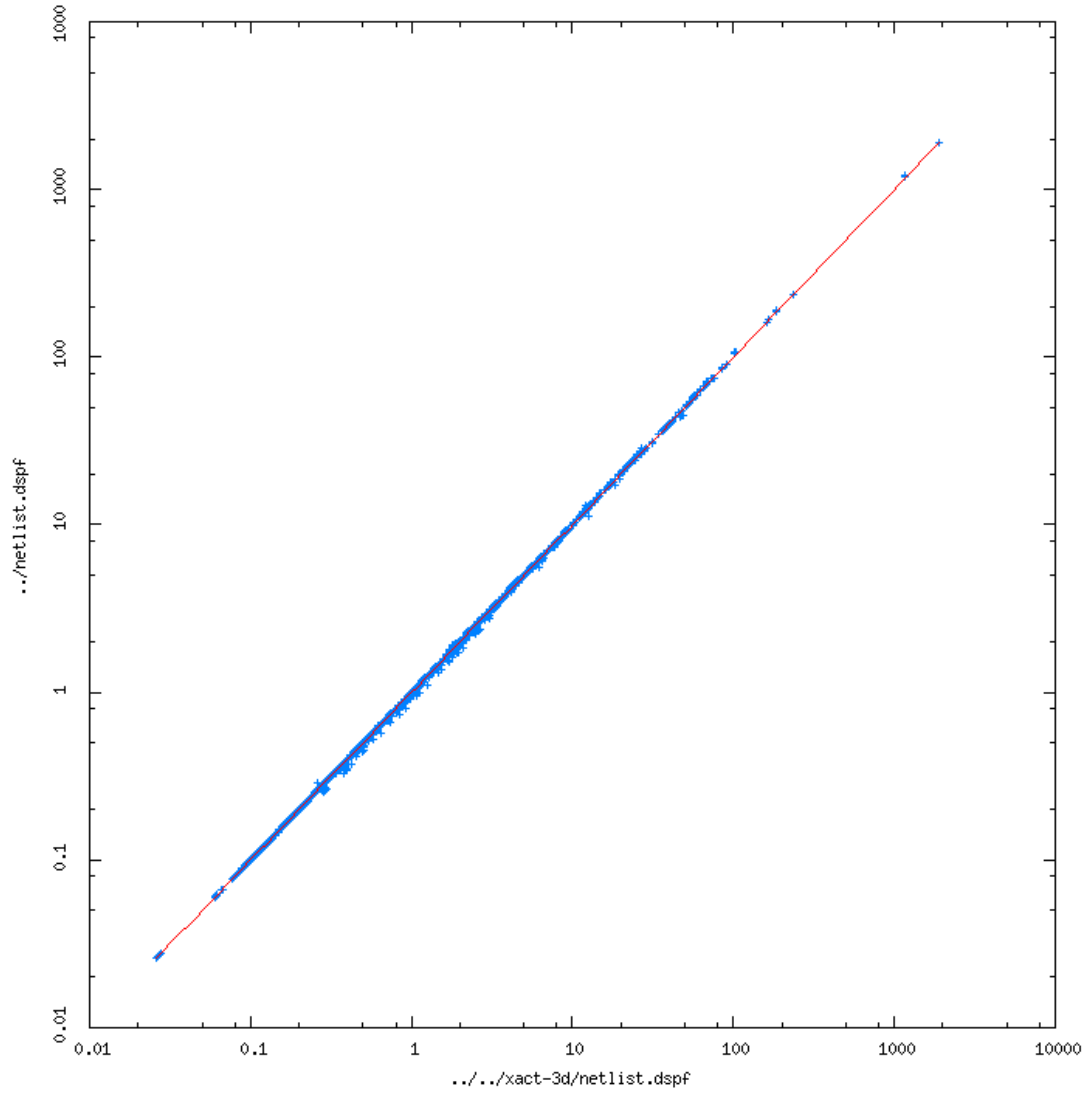


- Solves Maxwell's equations
- Highest accuracy

$$\vec{\nabla} \cdot \vec{E} = \frac{\rho}{\varepsilon} \qquad \vec{\nabla} \times \vec{E} = -\frac{\partial \vec{B}}{\partial t}$$

$$\vec{\nabla} \cdot \vec{B} = 0 \qquad \vec{\nabla} \times \vec{B} = \mu\varepsilon \frac{\partial \vec{E}}{\partial t}$$

Calibre xACT Accuracy
N16 customer testcase



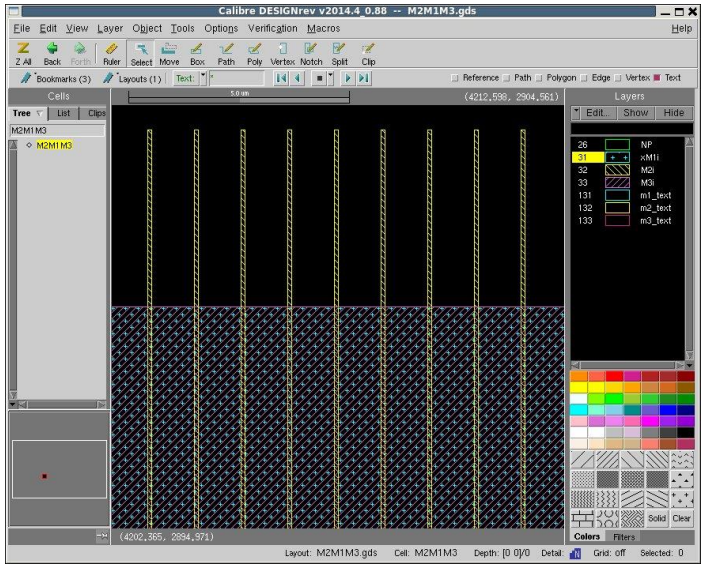
Calibre xACT vs. Calibre xACT 3D field solver	
Min	-13.1
Max	11.3
Mean	-0.1
Std dev	0.6

Filtered 5e-16

Calibre xACT Accuracy
Foundry test pattern vs. foundry golden

- All tools meet foundry qualification requirements

- Field solver has tighter standard deviation



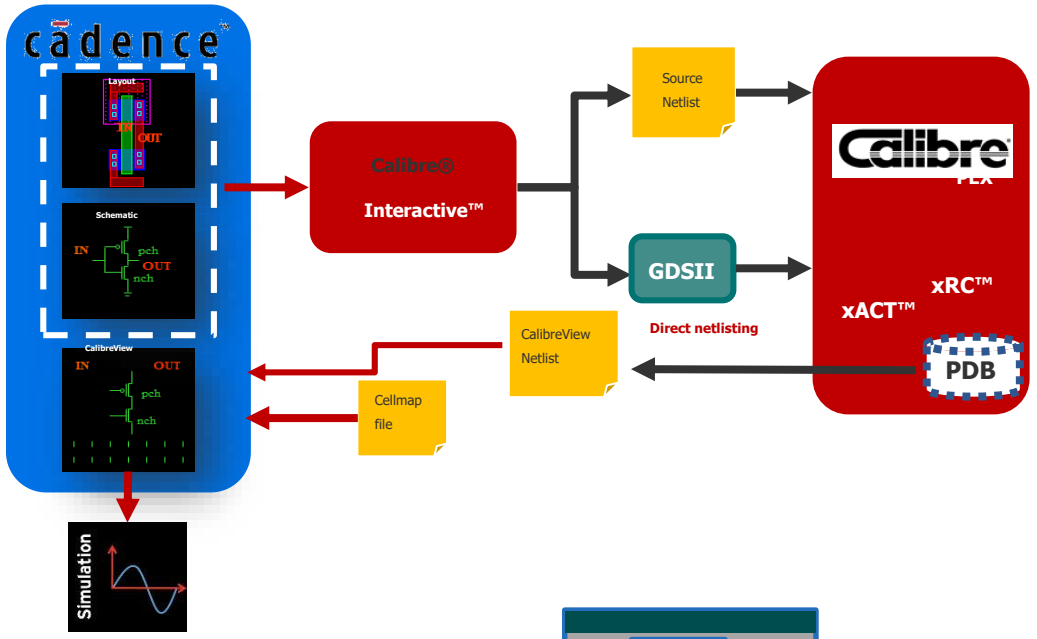
Metric	Calibre xACT	Calibre xACT 3D field solver
Min	-5.5	-3.9
Max	3.2	2.1
Mean	0.1	-0.2
Std dev	1.5	1.1

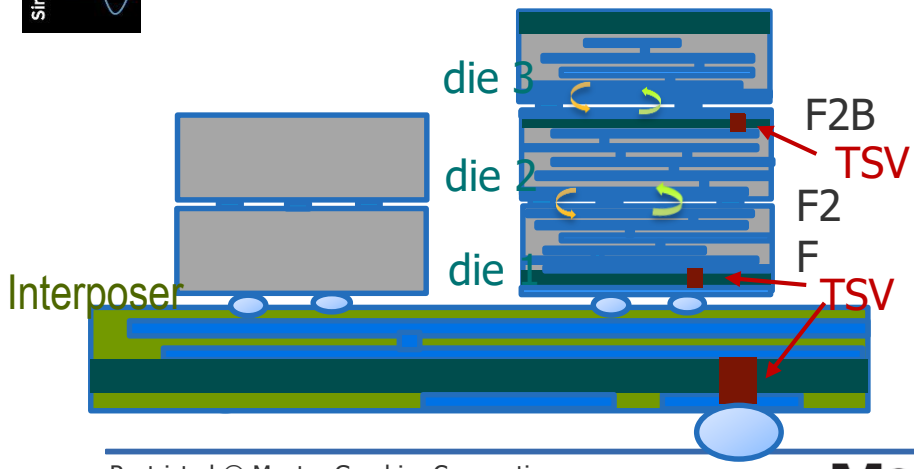
Calibre xACT Product Portfolio

- Calibre xACT – hybrid extraction engine – performance + accuracy for leading-edge, full-chip custom/analog/RF and digital design
- Calibre xACT 3D Field Solver – no-compromise, high performance field solver accuracy for memory and cell design
  - Order of magnitude faster than traditional FS
  - Repeatable, deterministic results (as opposed to statistical tools which have inherent error)
  - Capacity for multi-million transistor blocks
  - Common Calibre rule decks and use model
- Calibre xL – loop and partial inductance extraction for RF and high-performance design
  - Parasitic inductance associated with signal/return-path "loops"
  - Full chip inductance extraction of on-chip signal interconnects
  - Application in Analog and Digital design, Clock network, Transmission lines…
  - "PEEC" - selected critical nets extraction
  - Self partial inductance L and mutual inductance M for extracted for each conductor segment.
  - Application In RF/Analog critical signals, Differential Pairs, Small P/G nets...

Calibre xACT Flows And Applications

- Calibreview
  - Designers never have to leave the implementation cockpit
  - A Calibreview passes Calibre nmLVS and Calibre extracted parasitics to Cadence Virtuoso design environment
  - Contains the connectivity and intentional devices the Calibre LVS tool extracts, as well as parasitic devices extracted by Calibre PEX
- 3DIC extraction solutions for configurations including
  - Fan Out Wafer Level Processing (FOWLP)
  - Wafer on Wafer stacking (F2F and F2B)





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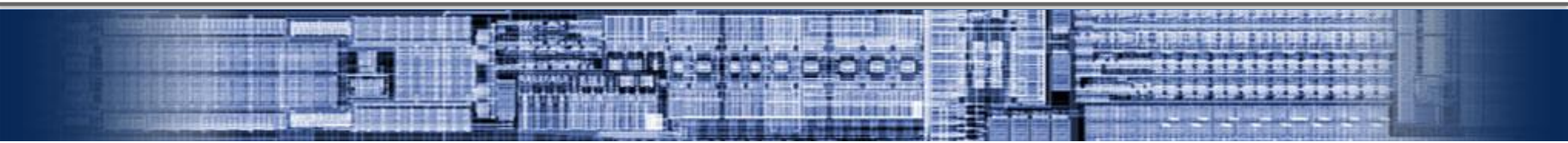
Silicon Creations



Developing Leading IP

Mentor® A Siemens Business

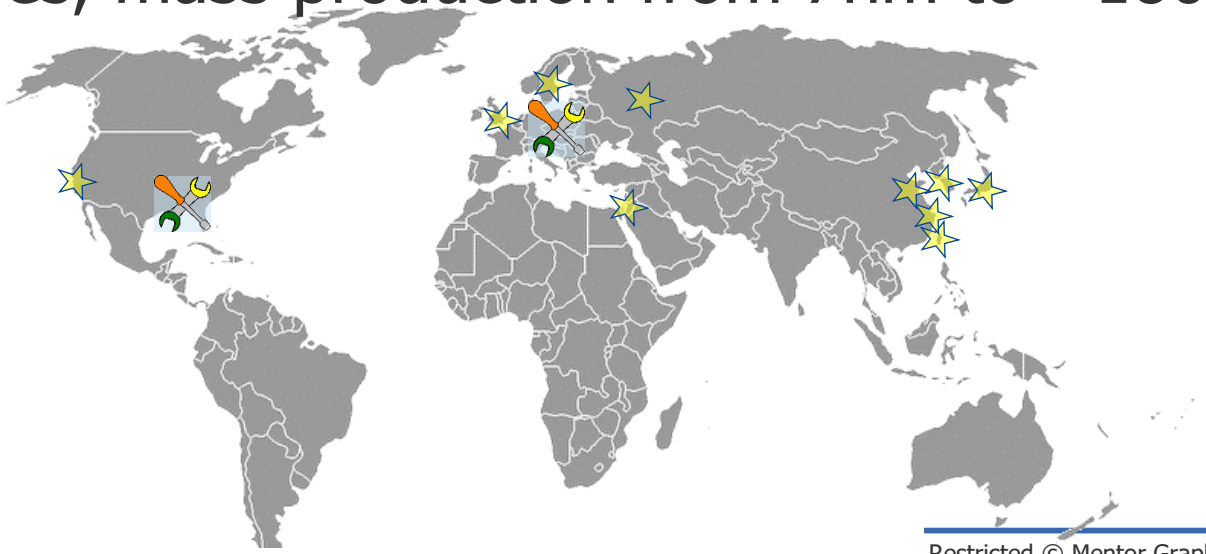
Agenda: Developing Leading IP

Collaboration between Silicon Creations and Mentor

- Introduction to Silicon Creations
- Challenges of developing PLLs & SerDes in advanced FinFET processes
- Using Calibre xACT and AFS for 5nm FinFET IP Development
- Silicon – Simulation correlations
- Summary/Q&A

Silicon Creations Overview

- IP provider of PLLs, Oscillators and High-speed Interfaces
- Founded 2006 – self-funded, profitable and growing
- Design offices in Atlanta and Krakow, Poland
- High quality development, award winning support
- >160 customers (>60 in China)
- Over 10 foundries, mass production from 7nm to >180nm, 5nm coming



Awards for quality & support

TSMC

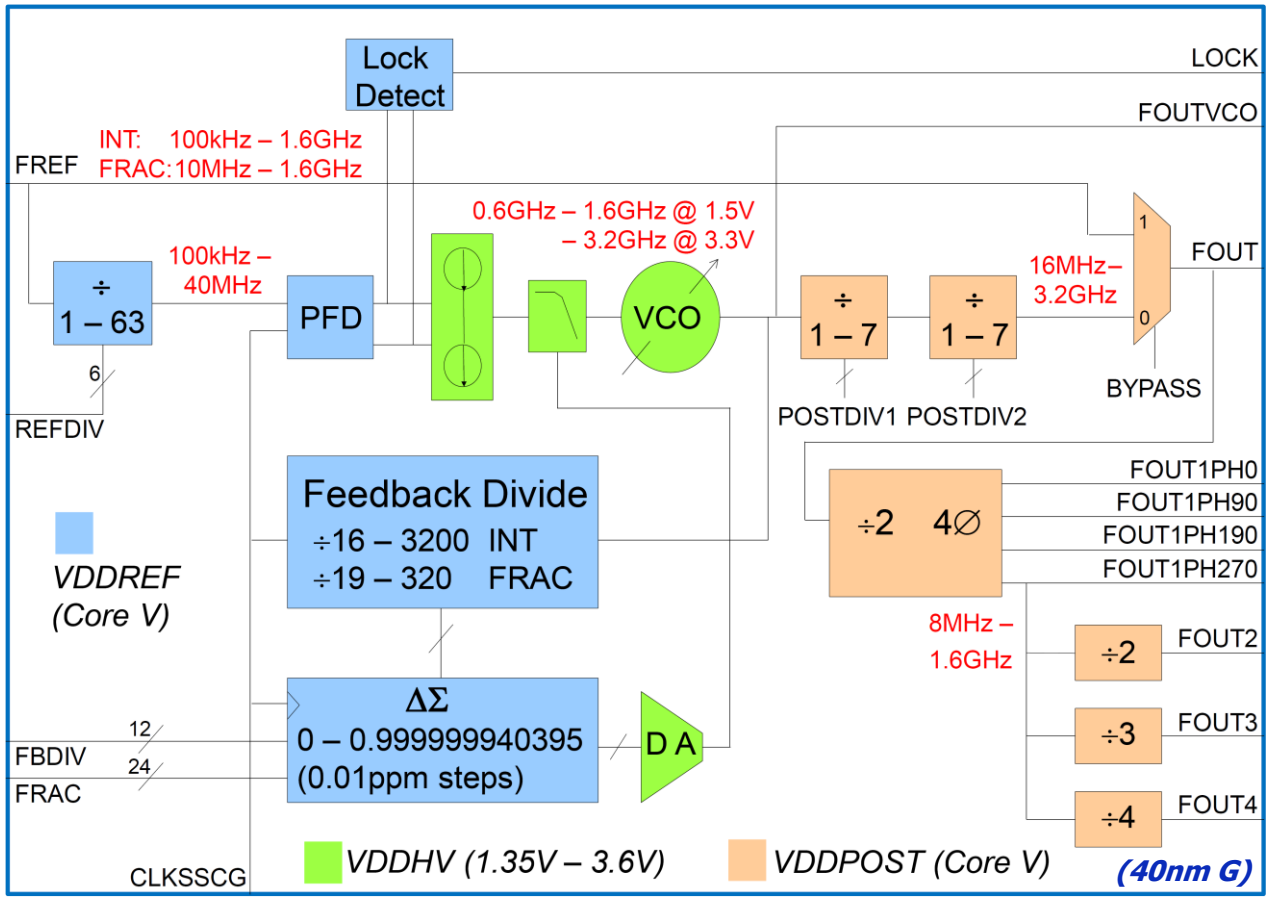
- 2017: Audience choice paper, USA OIP
- 2017: "Mixed-Signal IP Partner of the year"
- 2014: "Best Emerging IP vendor"

SMIC

- 2017 (no awards to anyone)
- 2015 & 2016: Best support
- 2014: Production volume growth
- 2013: Best Analog IP

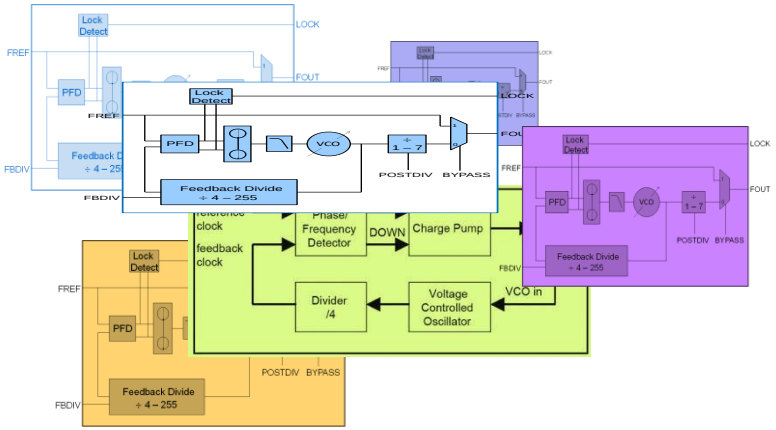
Fractional Ring PLL

- "One-Size-Fits-All" Synthesizer: flexibility reduces risk
  - Any crystal; <0.01ppm frequency step
- Programmable Power – Jitter Optimization
  - < 1mW
  - Long Term Jitter < 5ps RMS
- Production from 7nm – 180nm, 5nm in development
  >150 chips, > 1M wafers in 28nm
  > 40 chips, > 800k wafers in 16nm
- Derivative PLLs for
  - Core voltage only
  - Integer-only
  - Low area
  - Ultra-low jitter
  - Ultra-low power



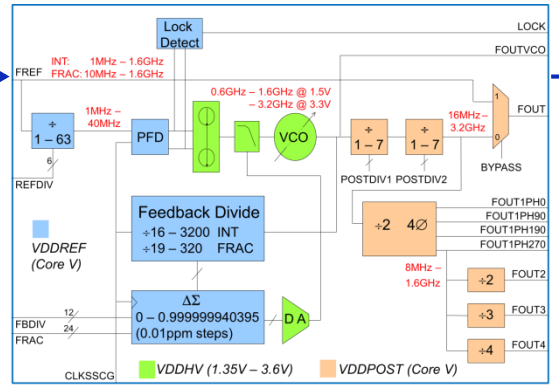
Why our Fractional PLL?

Competitor PLLs



Silicon Creations

1 to 1600 MHz



4 to 3200 MHz

Risky & expensive

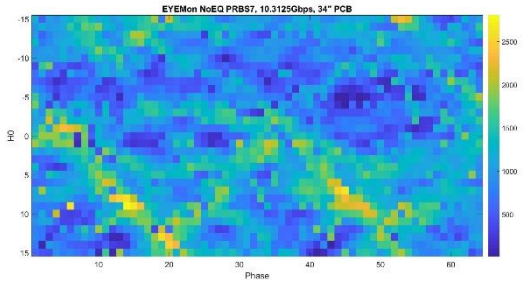
– Built new each time
– Narrow input/output ranges
  … new silicon to change
– Buy a new IP for every clock

Lower risk & lower cost

– Predictable, measured
– Wide range, programmable
  power-performance tradeoffs
– One PLL, many applications – save $, ¥, €
– Best support

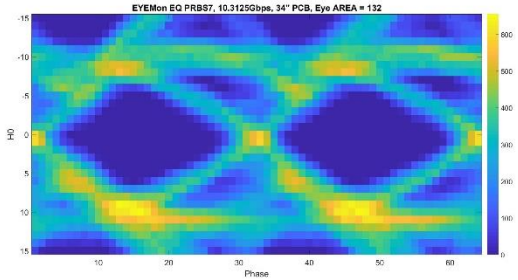
Multi-Protocol SerDes PMA

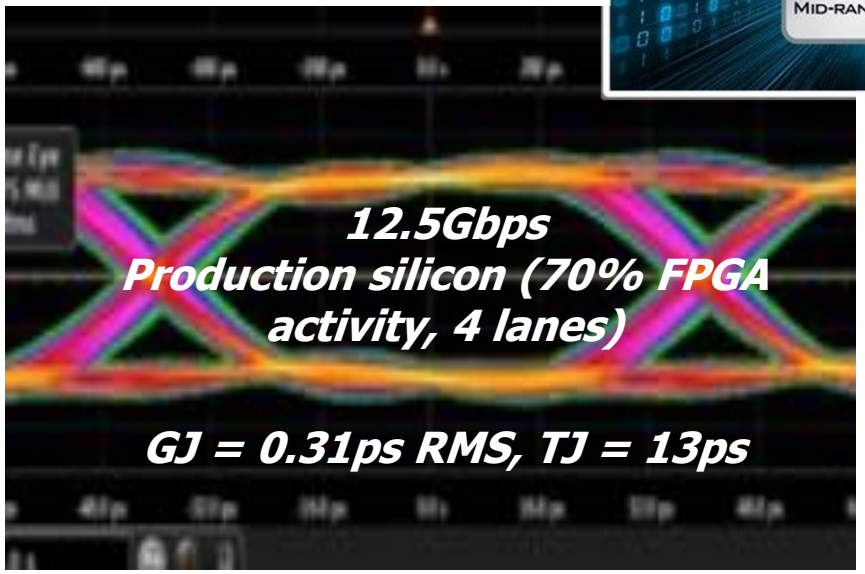
- 0.25 – 12.7Gbps SerDes PMA (28nm LP, 40 LP, 12FFC soon)
- Low Power (mW/Gpbs/lane): SR ~4.5mW, LR ~8.6mW
- Jitter cleaner Tx Ring PLL → Low Area



(10.3Gbps,
25dB channel loss)

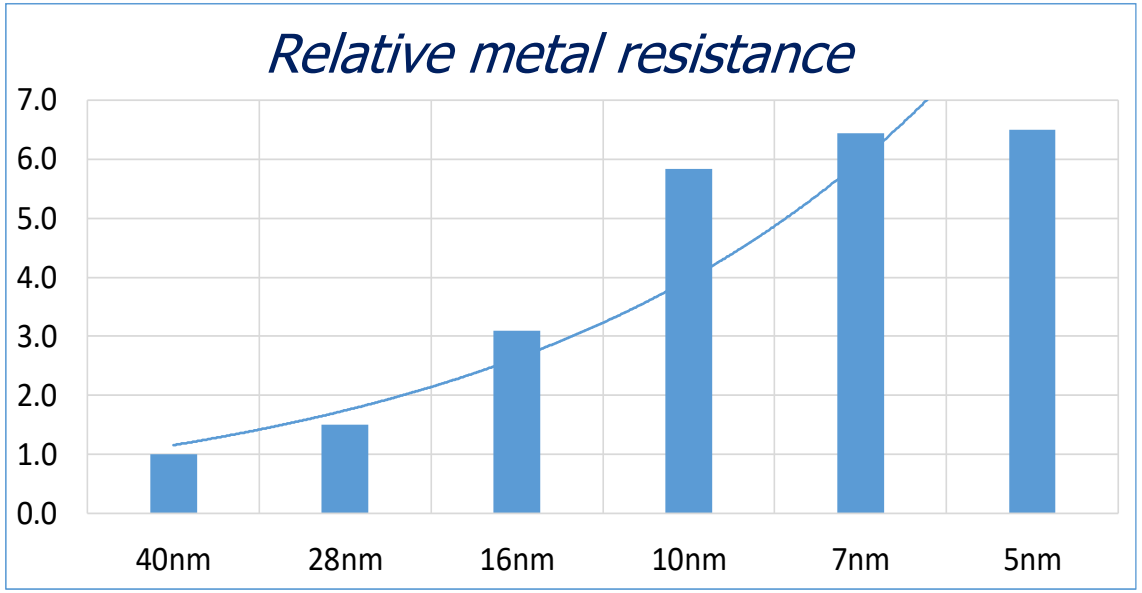
5-tap DFE + CTLE +
Eye monitor +
Adaptive Eq.
→ >30 protocols





Wire resistance challenge

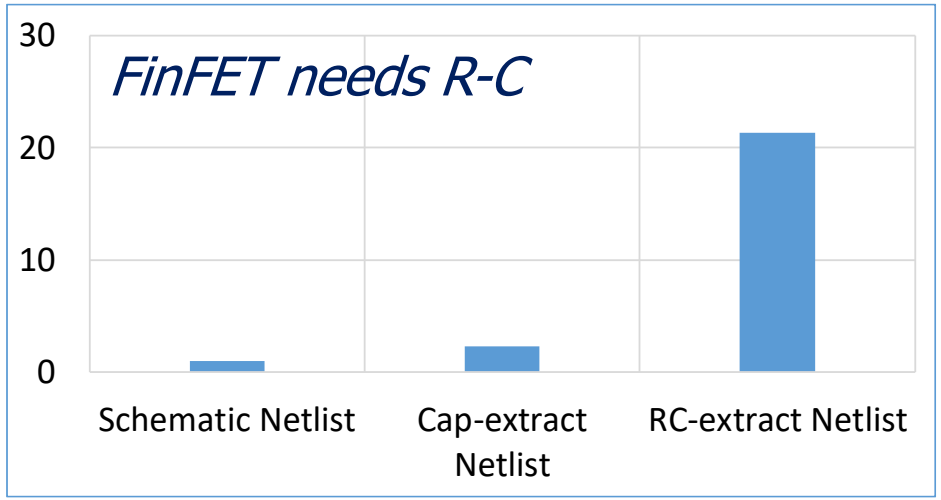
- Interconnect resistance is climbing quickly!
- Extraction and post extract simulations are becoming more important
- From 40nm to 5nm/7nm, wire resistance (Ω/sq) has risen ~6.5x
- Designs are increasingly difficult to verify due to the need for simulation of distributed RC parasitics

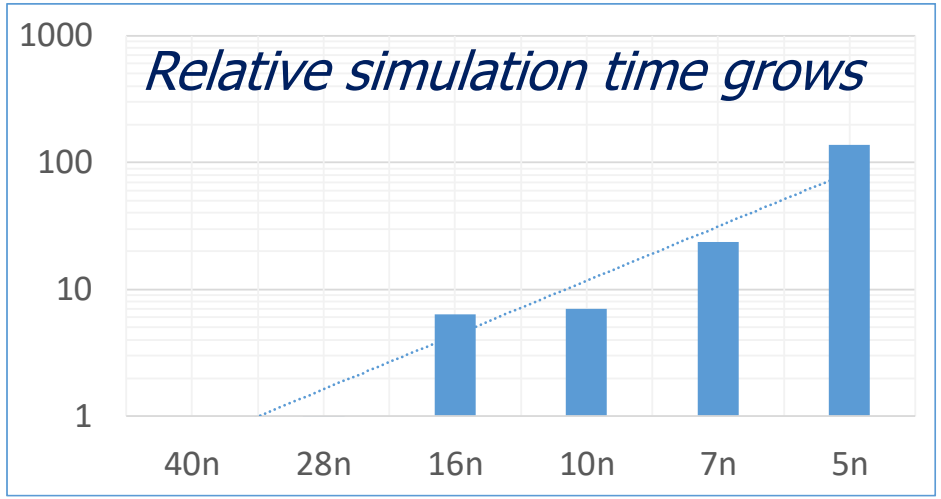


5nm Simulation Time

- Schematic sims are out, distributed C-C and R-C extracted simulations are essential
  - We use Calibre Xact to generate accurate netlists
- Models are becoming more complex

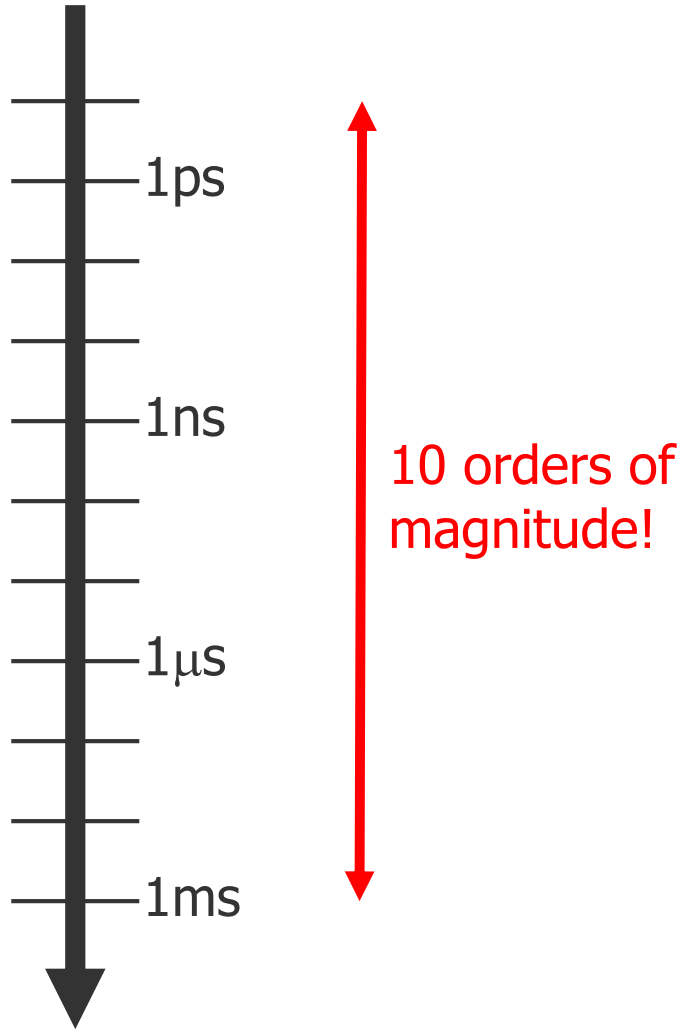
→ Higher development costs:
- Longer development cycles
- Need parallel simulation and more CPU's
- Need more EDA licenses





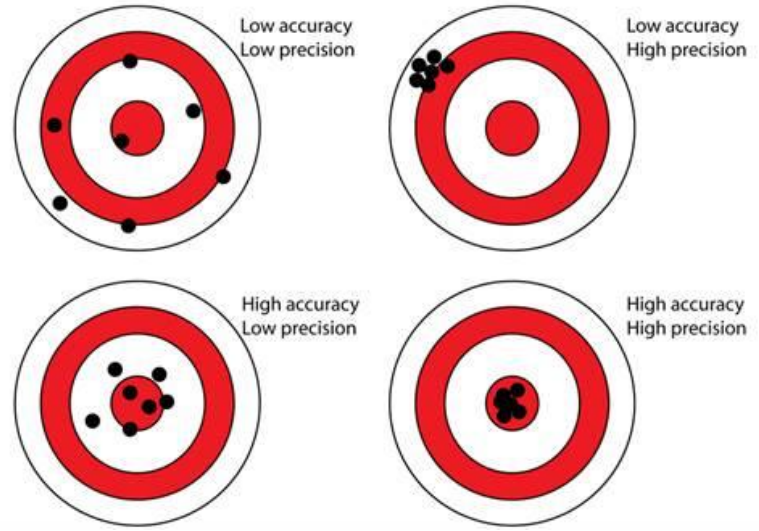
Simulation time scale
Makes things worse for PLLs & SerDes

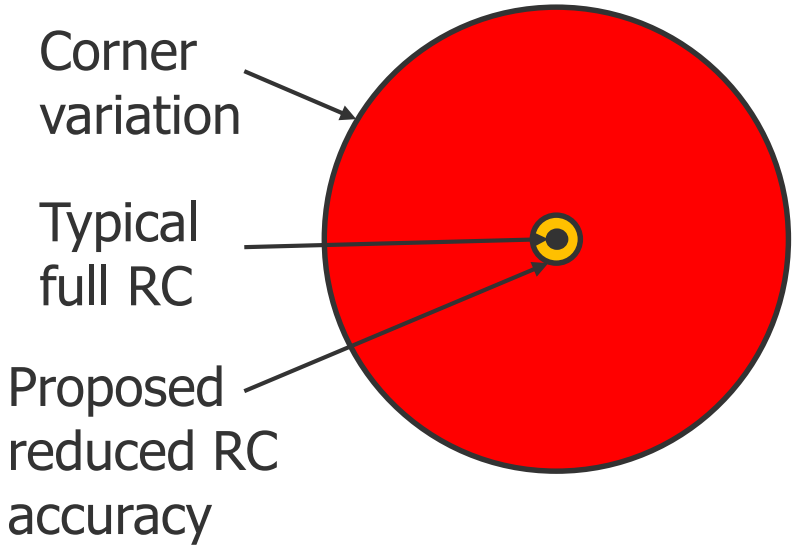
- Jitter requirements ~ 0.1ps
- Bit rates / clock cycle time ~100ps
- AC coupling time constant ~1µs
- PLL lock time ~50µs
- Link behavior ~1ms



RC Reduction and Accuracy

- RC reduction is one way to decrease simulation time (and cost!)
- Goal: reduce simulation time (lower cost), but preserve reasonable accuracy
- The corner spread can be used as a reference for what is reasonable
  - Corner spread is typically ~40%
  - Some precision can be lost without much effect on margin





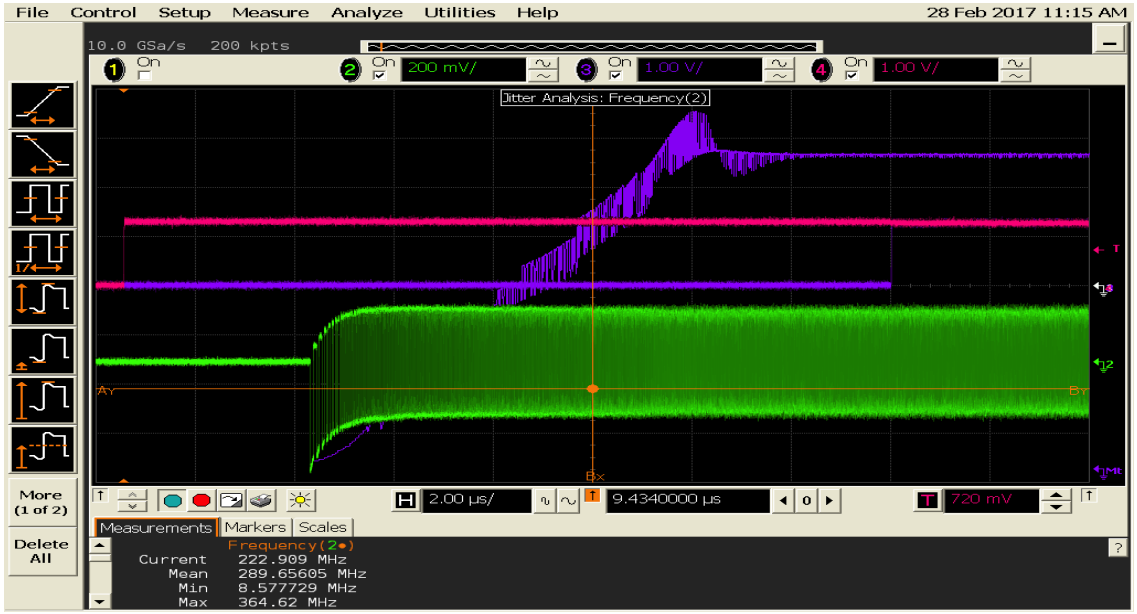
RC Reduction Example – 28nm VCO

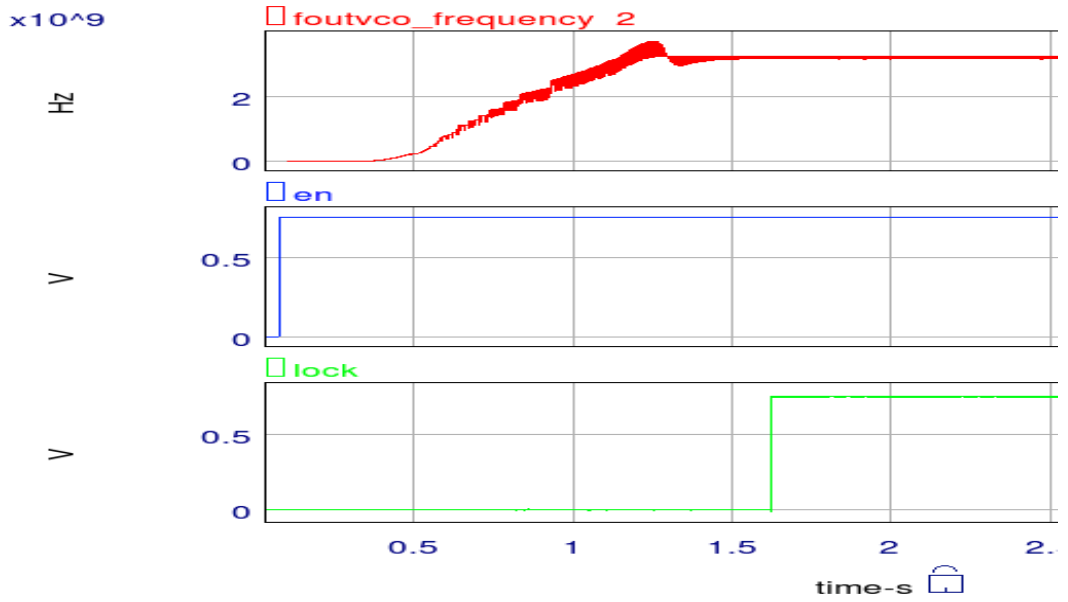
- Example:
  - compare full RC & reduced RC, CC & reduced CC
  - Look for accuracy, simulation time (cost)
- Full RC netlist used as the "gold standard"
- CC netlist runs in 1/10th the time, but at a 7% frequency error
- Highlighted strategy
  - Join R's < 1 Ohm, merge C's < 0.1fF
  - Total cost, in units of [token*seconds], is reduced 6x
  - Frequency error only ~0.1%
- Strategy and merge thresholds depend on block, process
  - significant time (cost) savings possible!

Simulation	Relative Frequency Error [%]	Relative Time [%]	AFS Tokens	Relative Cost [%]
RCC - gold stanard	0.000	100.0	2	100.0
RCC w/ 30GHz Tau reduction	0.024	91.3	2	91.3
RCC w/ 10GHz Tau reduction	0.024	90.9	2	90.9
RCC - join R < 0.1 Ohm, join C < 0.01 fF	0.004	52.2	2	52.2
RCC - join R < 1 Ohm, join C < 0.1 fF	0.125	34.8	1	17.4
CC only	6.909	10.4	1	5.2
CC only, join C < CABS 10%	5.554	9.4	1	4.7

7nm Area Optimized PLL Locking Simulation vs. Measurement

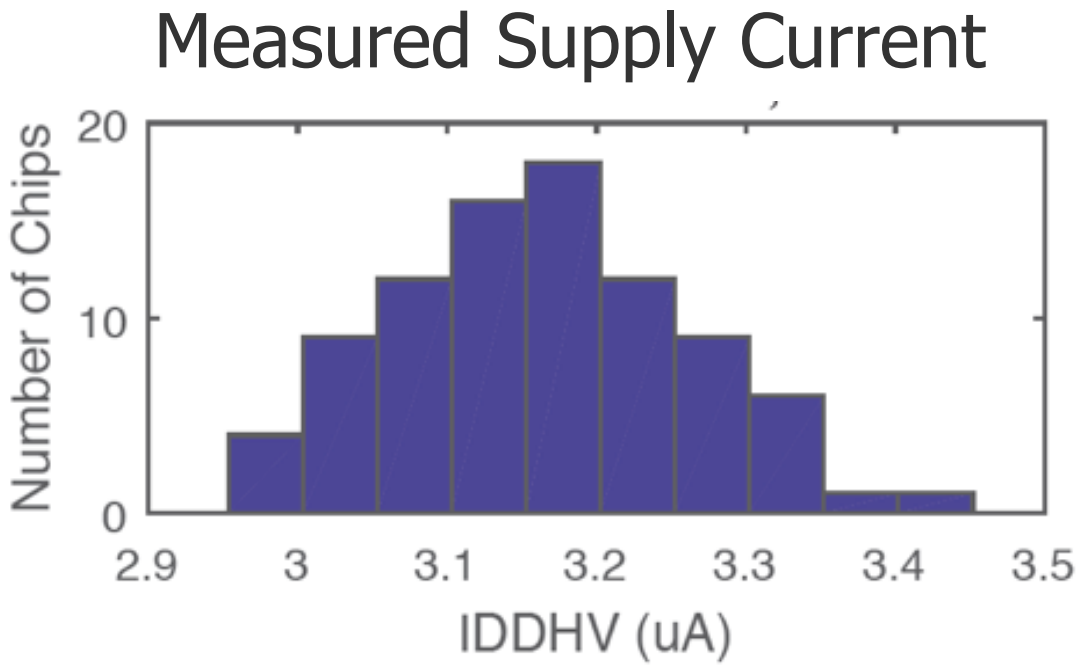
- Lowest area PLL for digital clocking – 0.009mm2
- Total power under 200µW
- Accurate netlist provides an excellent correlation between AFS transient simulation of frequency vs. time and silicon measurements





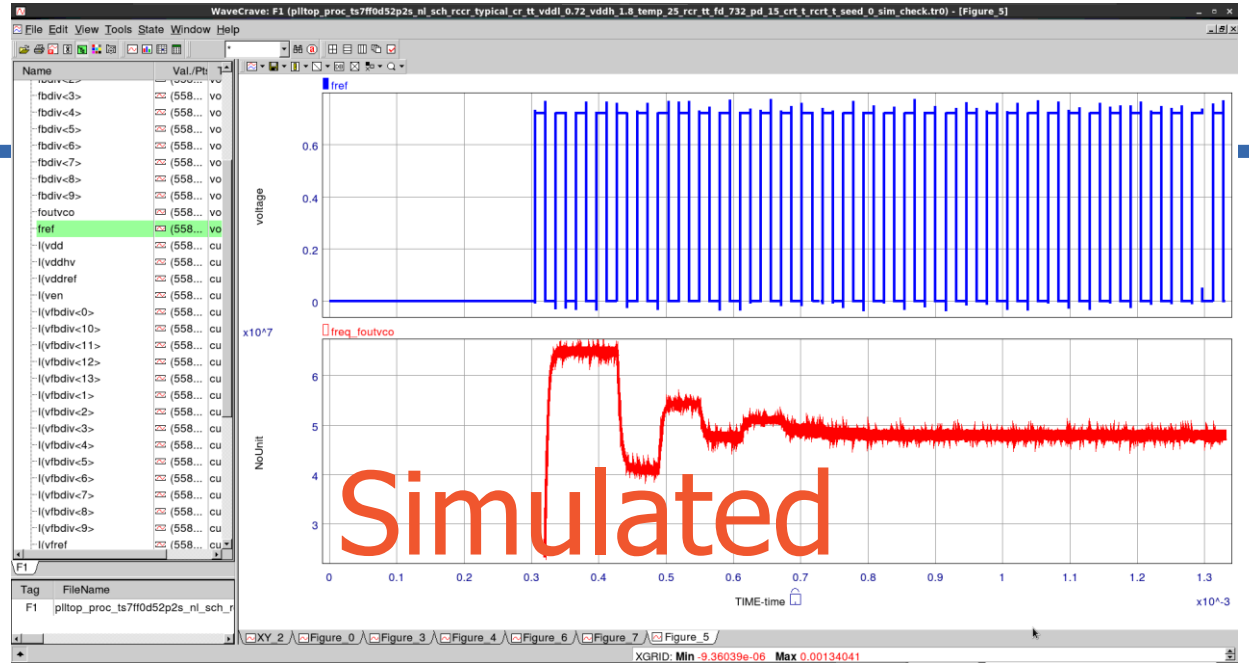
7nm IoT PLL Current Consumption
Accurate parasitics → first time right design

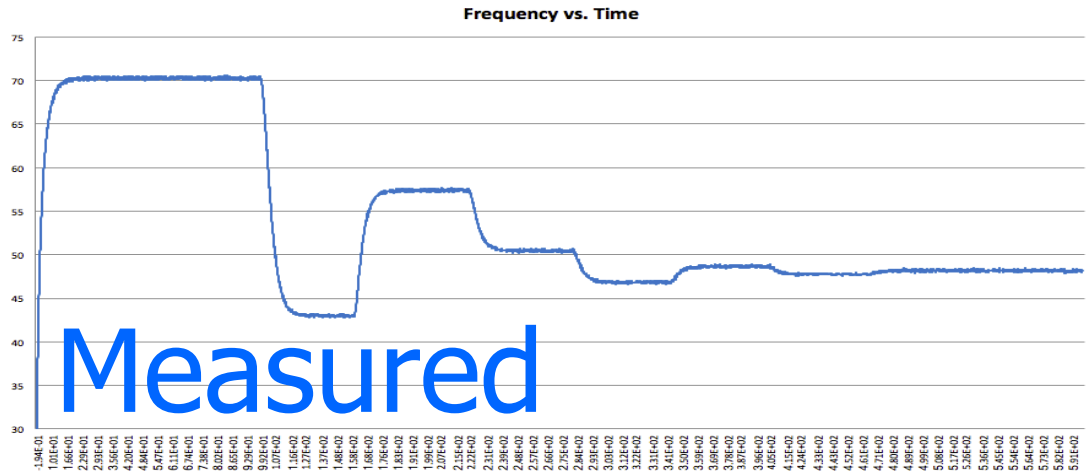
- **Simulation**
  - Mean=3.02uA
  - Stddev=1.5%
- **Measurement**
  - Mean=3.15uA
  - Stddev=1.6%



IoT PLL
Fast Locking

- AFS transient simulations accurately predict locking behavior (VCO frequency vs. time)
- 32kHz locking simulations must run for >1ms, so we need not only a fast locking PLL, but also
  - A fast simulator
  - Accurate netlist from Xact (carefully reduced)

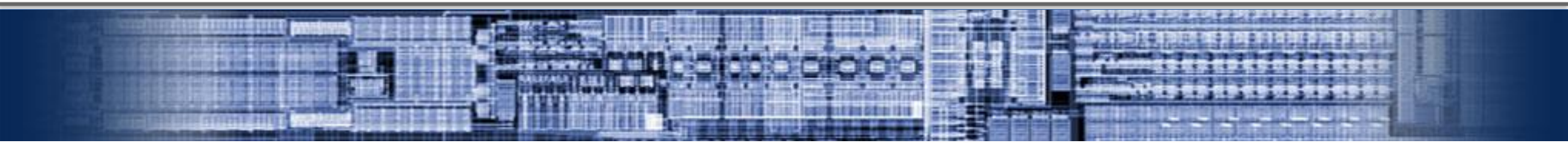




Silicon Creations Summary

- Key challenges for FinFET PLLs & SerDes
  - Necessarily long simulations due to tiny time steps and need to simulate a long time for loops to settle
  - High metal resistance requires distributed RC-extraction and netlist reduction if we want simulation results before the silicon comes back
- Solution
  - Really accurate extraction from Calibre Xact provides this
  - A powerful and fast simulator – Mentor AFS
- The reward – for us and our customers
  - 7nm low jitter PLLs and ultra-low power PLLs that go to production on first silicon

Silicon Creations



Thank you!

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