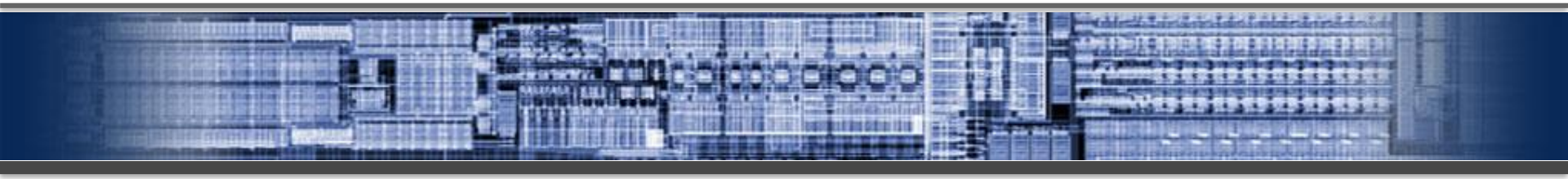


Validating performance of clocking systems using microwatts of system power from 180nm to FinFET

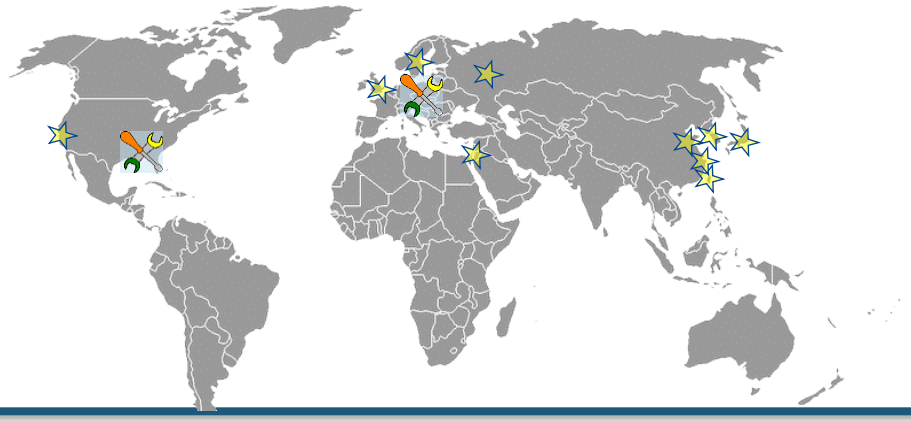
Andrew Cole, VP at Silicon Creations

Outline

- Silicon Creations introduction
- PLL optimizations … extreme low energy for IoT
- Challenges of doing this in advanced FinFET
- Correlating Simulation and Silicon Results
- Summary

Silicon Creations Overview

- IP provider of PLLs, Oscillators and High-speed Interface
- Founded 2006 – self-funded, profitable and growing
- Design offices in Atlanta and Krakow, Poland
- High quality development, award winning support
- Mass production from 7nm to >180nm, 5nm taped out

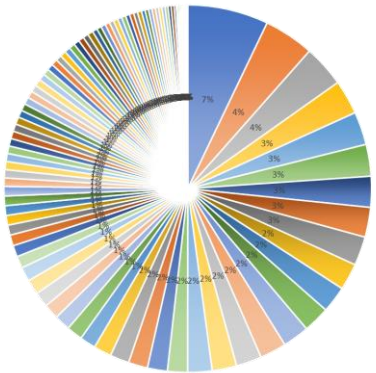


Some statistics

> 190 customers … Growing at >3/month

> 300 IP products … Growing at >4/month

> 500 chips in production using our IP…
Growing at 5 to 10/month

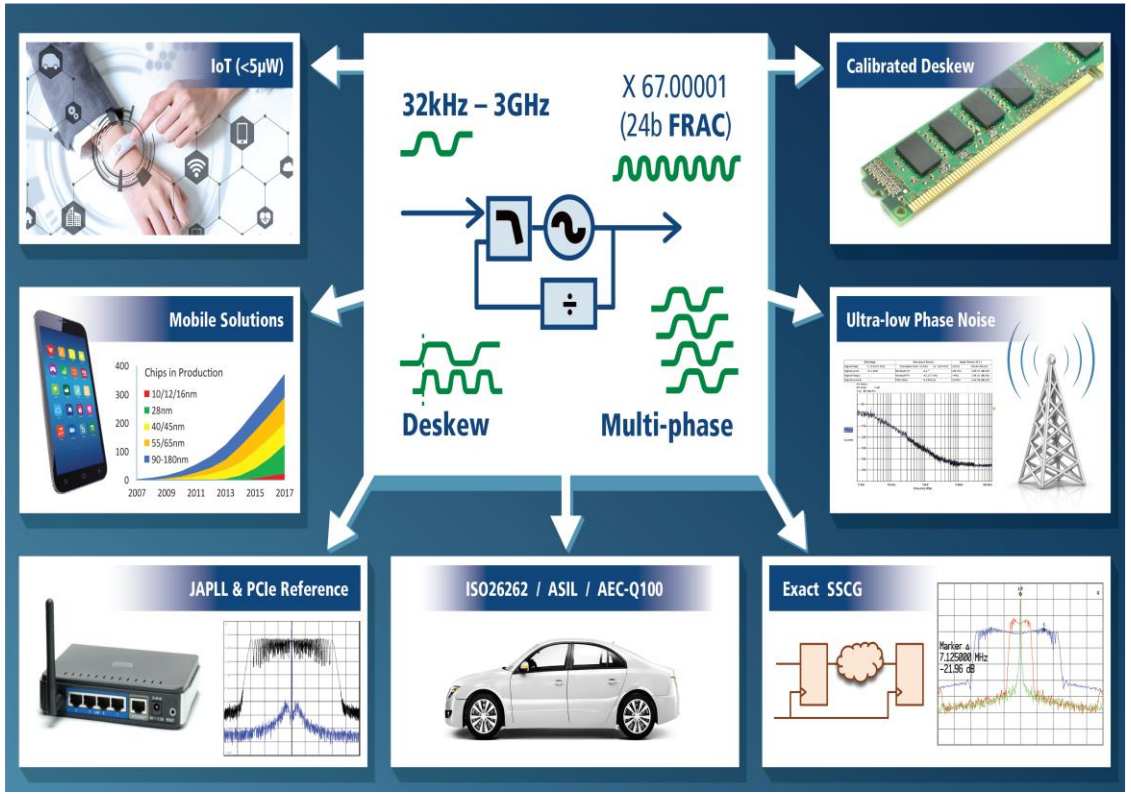


Income from >95customers in 2018
… we don't depend on any one customer and will be here when you need us to be

PLLs from Silicon Creations

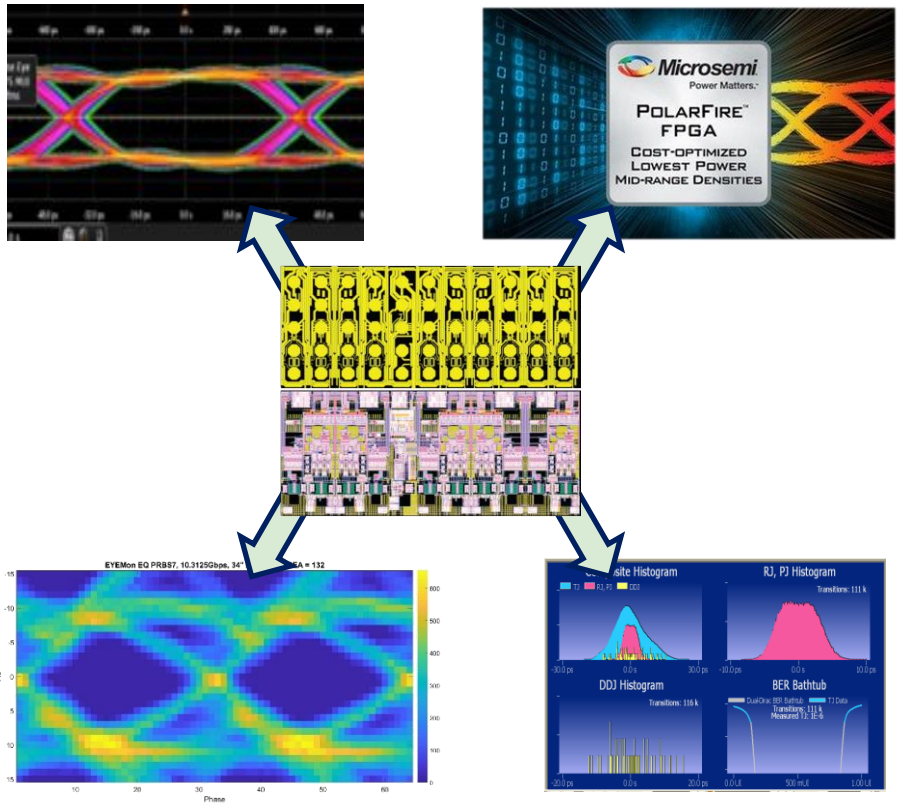
- Highest volume analog IPs – robust design and good QA are essential
  e.g. Fractional-N PLL:
  > 300 MP chips
  > 3M wafers
  … Many B's of these PLLs produced

- PLL products include general purpose, fractional, low jitter AFE, μW IoT, Automotive



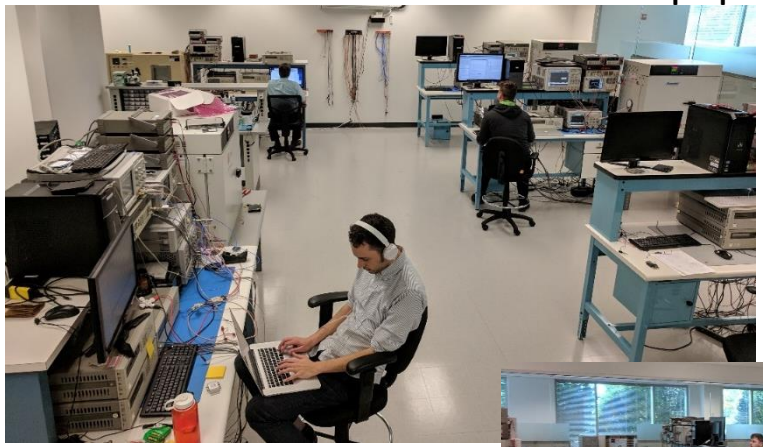
SerDes from Silicon Creations

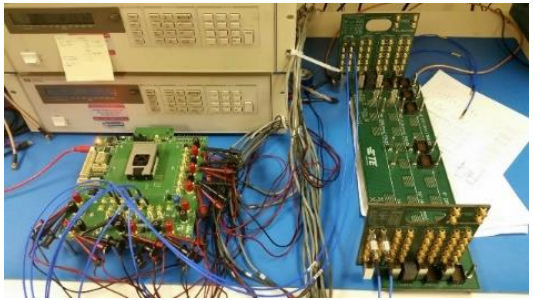
- Robust and proven from 28nm to 180nm and from <100Mbps to >20Gbps
- Multiprotocol (for FPGA) and targeted protocols
  - SGMII, XAUI, RapidIO, V-by-1 HS/US, FastLVDS, CameraLink, FPDLink, OIF-CEI, JESD204, CPRI, PCIe1-3, 10G-KR, …
- Come to our booth to learn more



Lab Testing

Test lab with Matlab controlled equipment – 12 benches





> 100 IP test reports from 7nm to 180nm

Awards for quality & support

TSMC

- 2018 & 2017: “Mixed-Signal IP Partner of the year”
- 2017: “Audience choice paper” – USA OIP
- 2014: “Best Emerging IP vendor”

Awards for quality & support

SMIC

- 2017: (no awards to any)
- 2015 & 2016: Best support
- 2014: Production volume growth
- 2013: Best Analog IP

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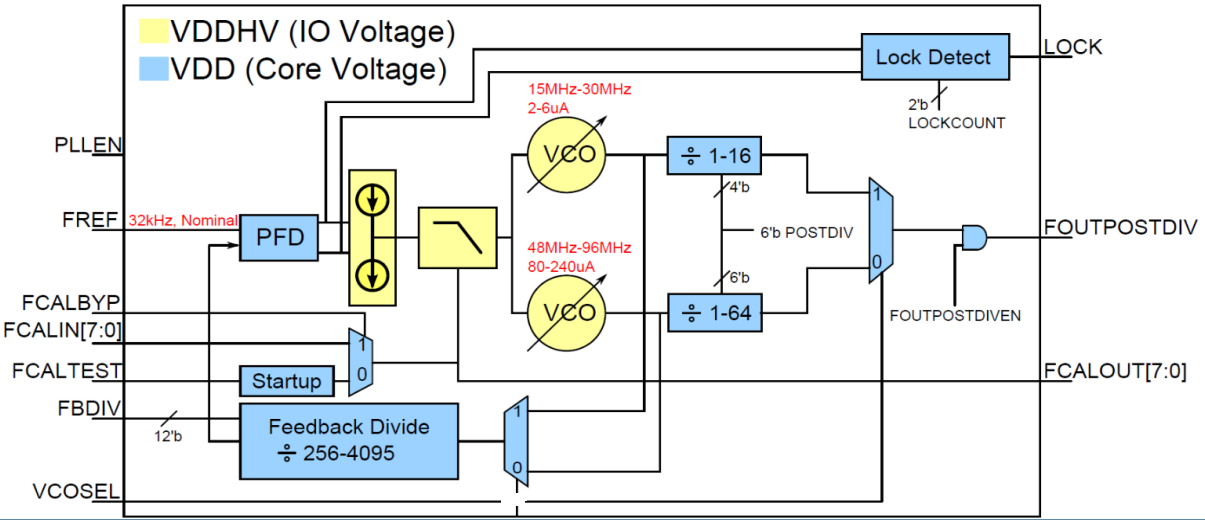
Clocking for “IoT”

- IoT = overused term, but useful shorthand for ultra-low power SoCs with
  - Low operating power
  - Able to start/stop quickly for low system power
  - Low leakage
  - Few/no external components

- Our clocking solutions use low-power process offerings:
  - 180nm, 40nm, 28nm and FinFET from 16nm to 7nm
  - PLLs with total power as low as 5µW and starting in as little as 3 reference clock cycles
  - Free-running oscillators with <2% total variation

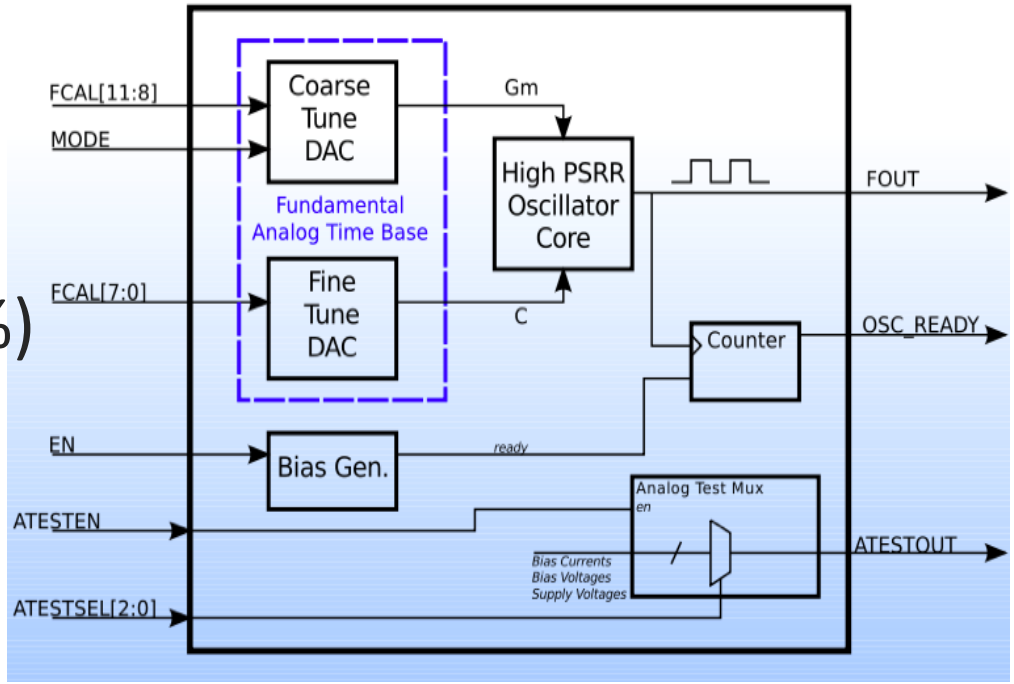
IoT PLL

- Extremely low power 32kHz RTC reference clock, as low as 5uW for whole PLL
- Starting – ±2% of freq. Cold in <1.2ms (40 cycles); Warm < 100us (3 cycles)
- 0.12mm2 and no external components
- Can include two VCOs – ultra-low power and decent jitter
- Production in planar from 180nm to 28nm and in FinFET from 16nm to 7nm



Free-running Oscillators

- Applications – watchdog timer, logic clock for ultra-low power mode (“IoT”)
- No external components
- Possible:
  (-40°C to 125°C, Vdd ±10%)
  - ±1.5% after trimming
  - Power < 30uW



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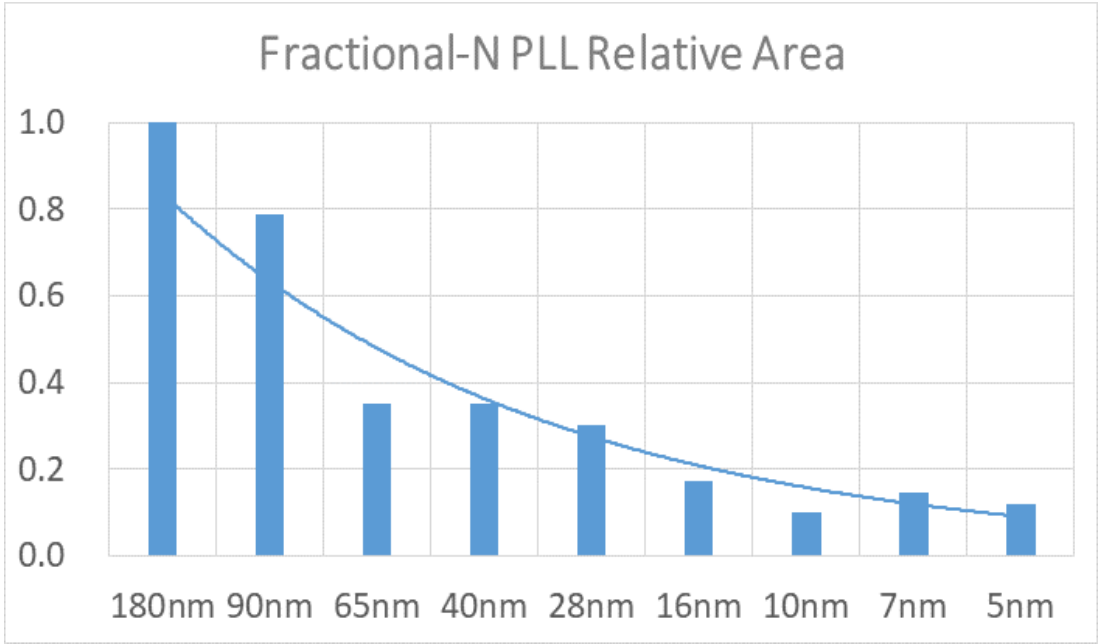
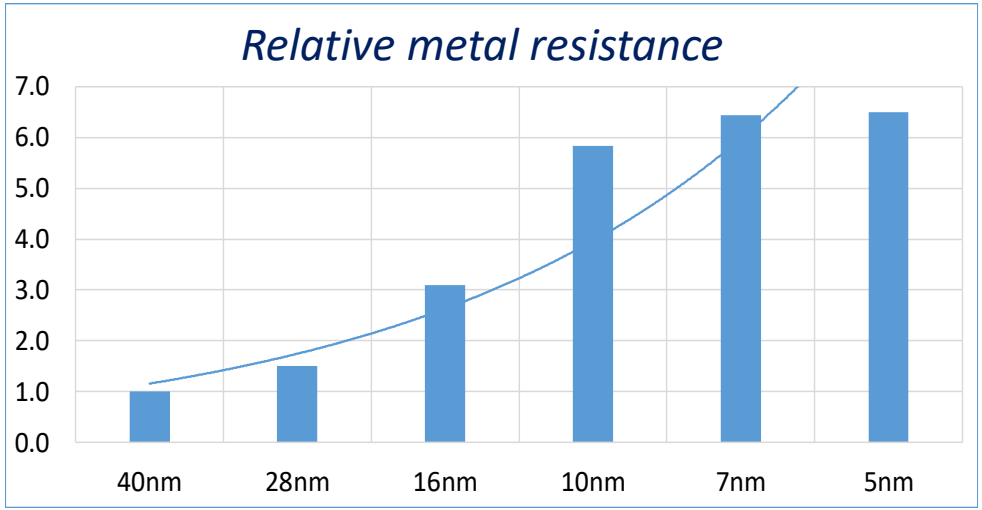
Analog scaling to 5nm

- Analog noise relates to kT/C, so area should scale with capacitance area
- It does! Analog scales, but less than digital
- From 180nm to 5nm:
  - Digital scaling ~800:1
  - Analog scaling ~8:1



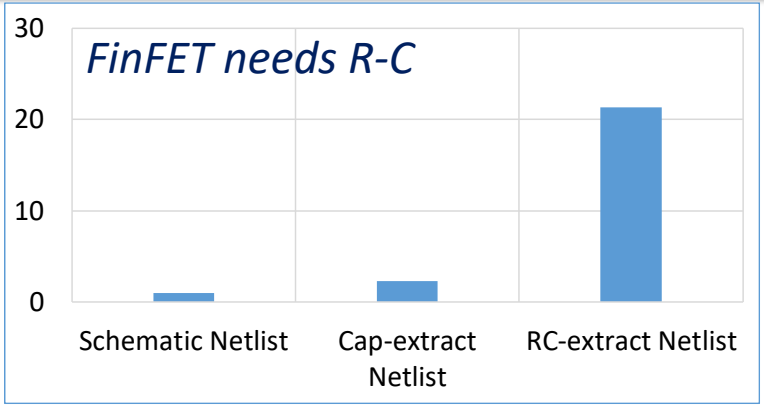
Wire resistance challenge

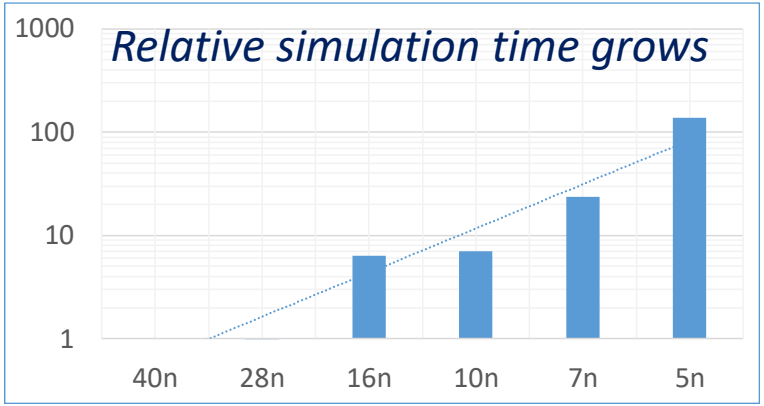
- Interconnect resistance is climbing quickly!
- Extraction and post extract simulations are becoming more important
- From 40nm to 5nm/7nm, wire resistance (Ω/sq) has risen ~6.5x
- Designs are increasingly difficult to verify due to the need for simulation of distributed RC parasitics



5nm Simulation Time

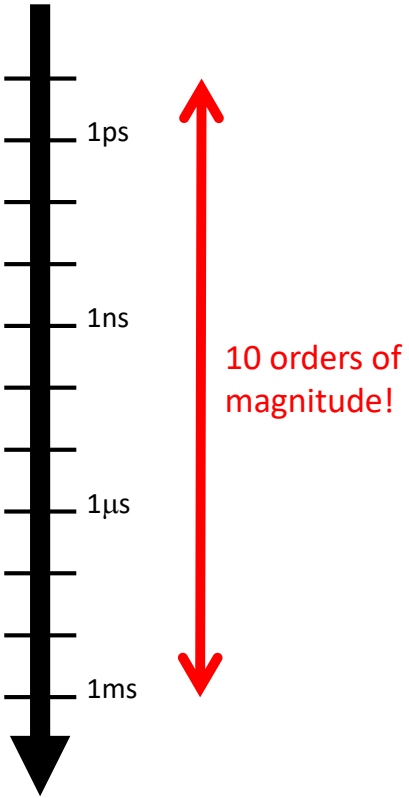
- Schematic simulations not good enough, distributed C-C and R-C extracted simulations are essential
- Models are also becoming more complex
  → Higher development costs:
  - Longer development cycles
  - Need parallel simulation and more CPU's
  - Need more EDA licenses





Timescale makes it worse

- Jitter requirements ~ 0.1ps
- Bit rates / clock cycle time ~100ps
- AC coupling time constant ~1us
- PLL lock time ~50us
- Link behavior ~1ms



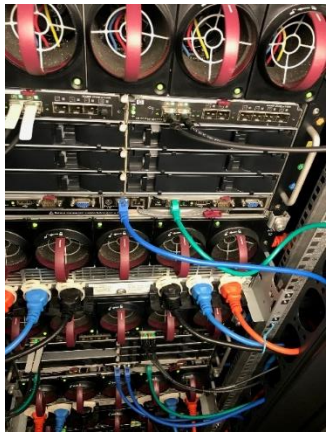
RC Reduction

- Example (28nm VCO):
  - compare full RC & reduced RC, CC & reduced CC
  - Look for accuracy, simulation time (cost)
- The right strategy/merge thresholds depend on kind of circuit and process technology

RC reduction strategy	Frequency error	Simulation cost
Distributed R-C-C (reference)	0.0%	100%
Distributed C-C	6.9%	5.2%
R-C-C, join R < 0.1Ω & C < 0.01fF	0.004%	52%
R-C-C, join R < 1Ω & C < 0.1fF	0.13%	17%

5nm Computing Solution

- Distributed computing
  - >2200 CPU cores
  - >15TB RAM
- 1200 Simulation licenses
  - 200+ 16-core extracted sims
  - 300+ 4-core extracted sims
- Dedicated Calibre machines
  - Intel i9-7980XE 18-core 4.8GHz
  - CPU de-capped, liquid-cooled
  - 4 x 16GB DDR4 RAM
- 15 Ton (140kW) Cooling



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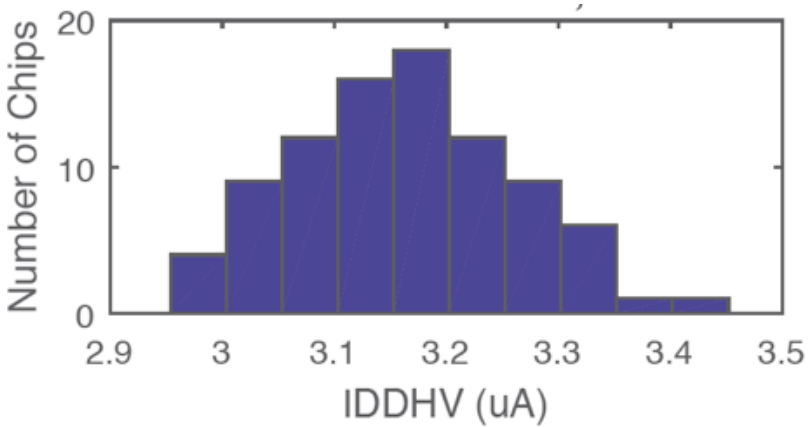
IoT PLL Power

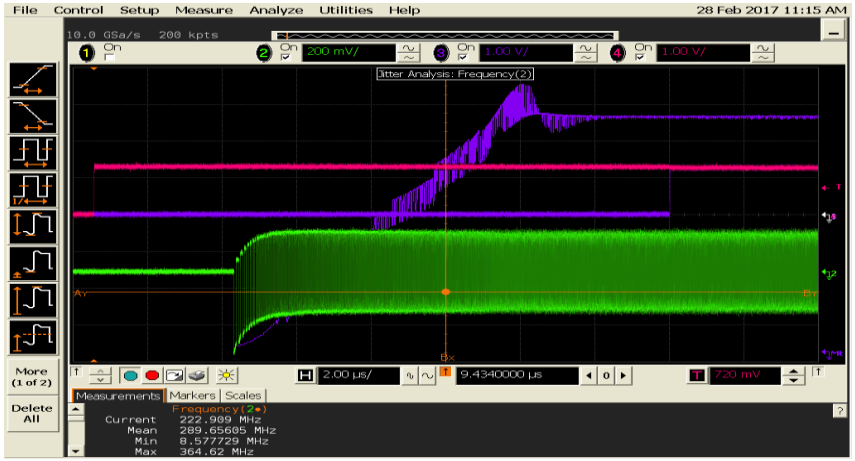
- **Simulation**
  - Mean=3.02uA
  - Stddev=1.5%
- **Measurement**
  - Mean=3.15uA
  - Stddev=1.6%

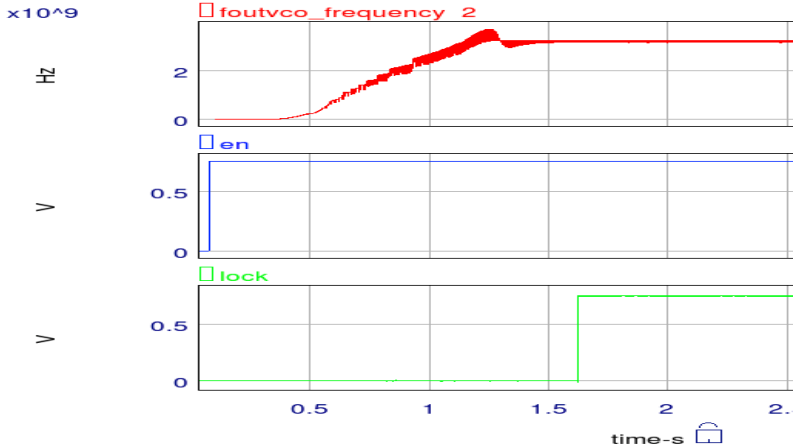
Measured Supply Current



7nm Low-Area PLL Locking

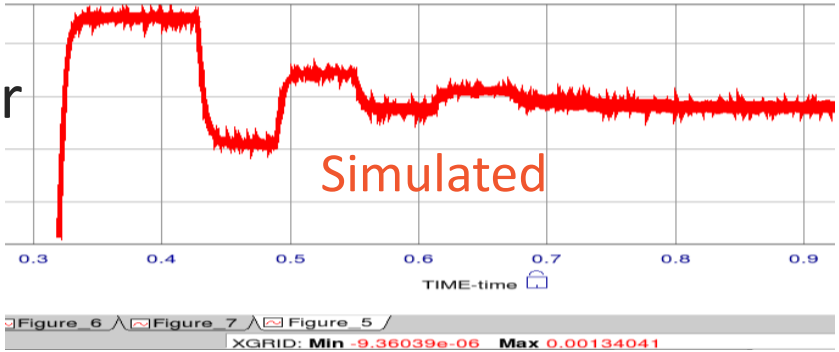
- Lowest area PLL for digital clocking – 0.009mm2
- Total power under 200µW
- Accurate netlist provides an excellent correlation between AFS transient simulation of frequency vs. time and silicon measurements

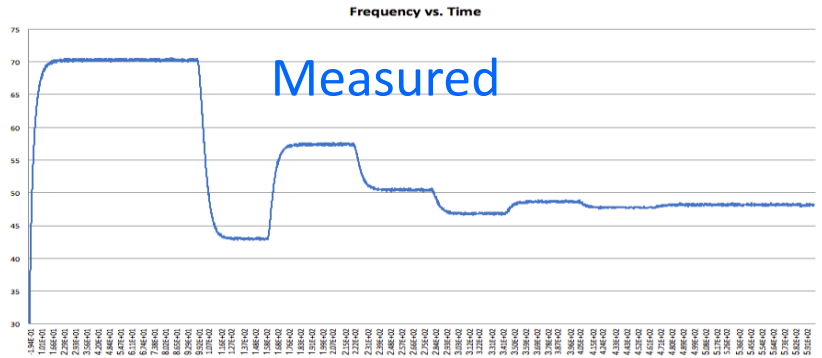




IoT PLL Fast Locking

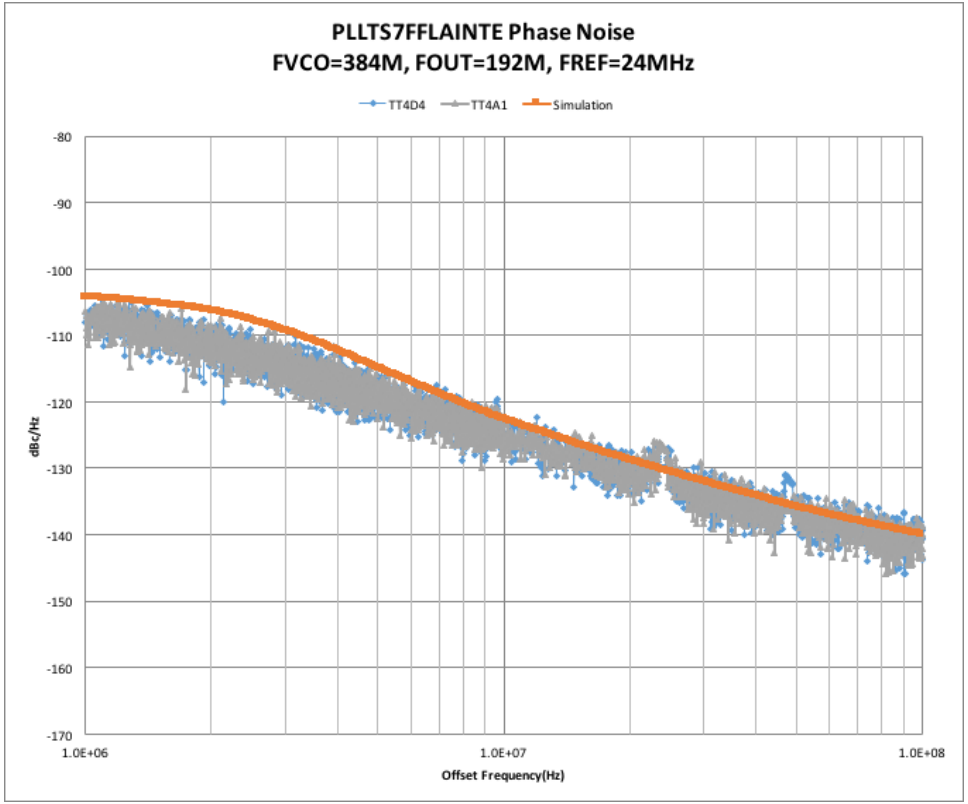
- AFS transient simulations accurately predict locking behavior (VCO frequency vs. time)
- 32kHz locking simulations must run for >1ms, so we need not only a fast locking PLL, but also
  - A fast simulator
  - Good SPICE models
  - Accurate extracted netlist (carefully reduced)





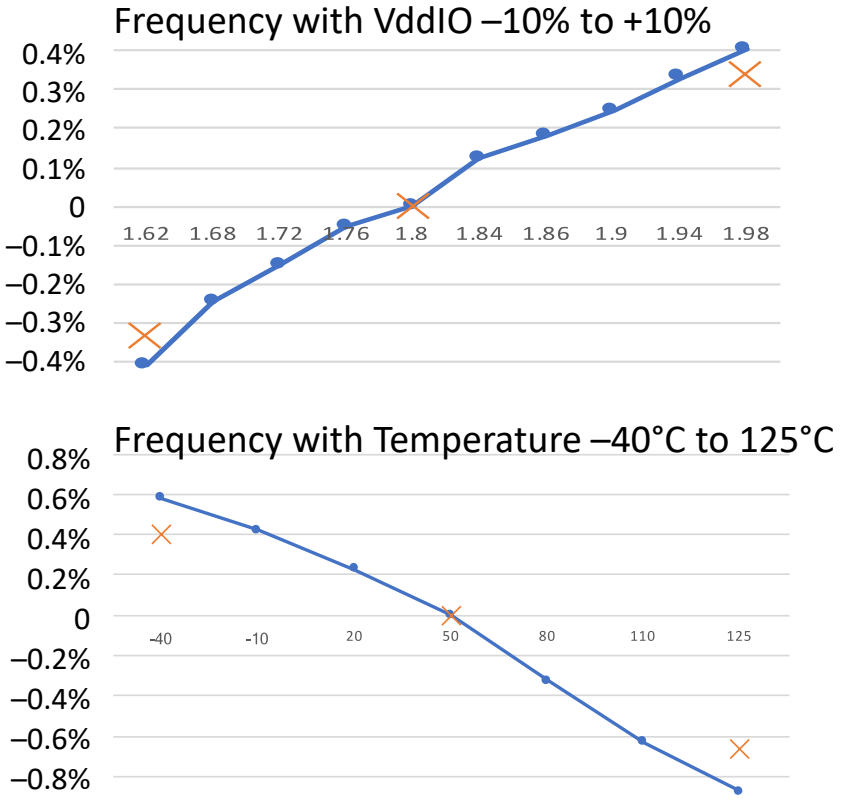
Phase Noise Correlation

- Ultra-Low Power (<100µW), Fast Locking PLL
- Phase noise (jitter) correlation achieved for PLLs with power from ~3µA to ~3mA



Oscillator Stability

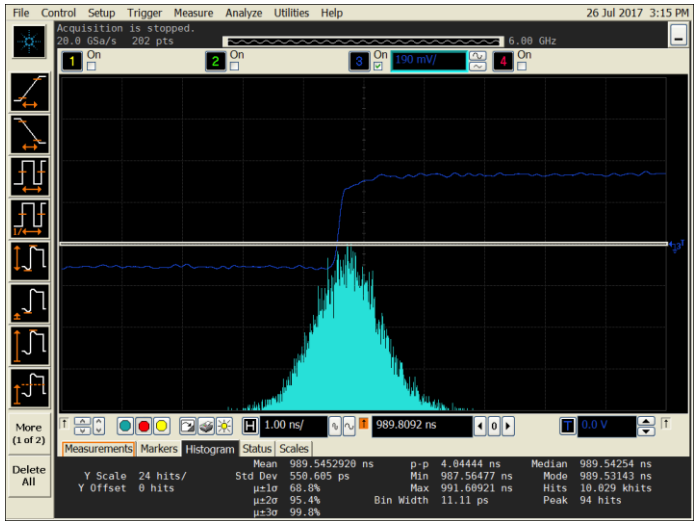
- Accurate frequency (without a crystal reference) across Voltage and Temperature variations



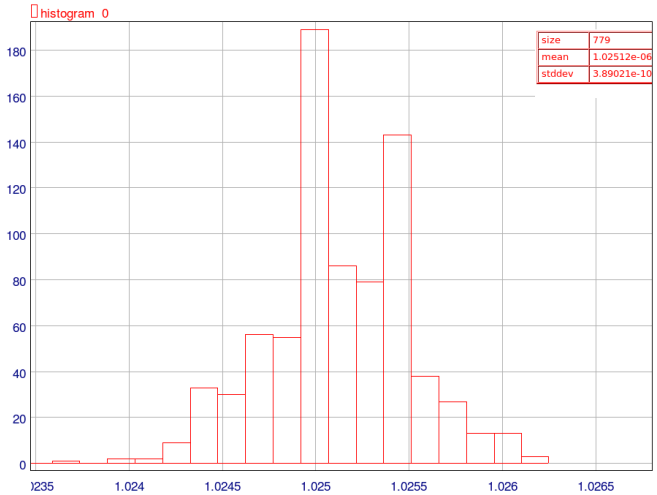
Oscillator Noise Correlation

- Highly non-linear, ultra-low power (<100µW), free-running oscillator is accurately modeled with AFS Transient Noise analysis

Measured OSCTS7FFRLXB – 0.55ns RMS



Simulated OSCTS7FFRLXB AFS Trannoise Analysis: 0.39ns RMS



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Summary

- Silicon Creations has been providing reliable, high performance clocking and SerDes solutions since 2006
- Designing in advanced FinFET nodes challenging and expensive
- With care, excellent correlations between simulations and first silicon have been shown in 7nm allowing production to start quickly
- Clocking solutions optimized for IoT contribute only a few uW to system energy and can be turned on and off quickly, yet can be designed for the target jitter
- 5nm solutions are taping out shortly